

Enhanced ESD, 3.0 kV rms/5.0 kV rms 200Mbps Quad-Channel Digital Isolators

FEATURES

- Ultra-low power consumption (1Mbps): 0.58mA/Channel
- High data rate: 200Mbps
- High common-mode transient immunity:
 - ADuM130x: 75 kV/ μ s typical
 - ADuM140x: 120 kV/ μ s typical
- High robustness to radiated and conducted noise
- Low propagation delay: 9 ns typical
- Isolation voltages:
 - ADuM130x: AC 3000Vrms
 - ADuM140x: AC 5000Vrms
- High ESD rating:
 - ESDA/JEDEC JS-001-2017
 - Human body model (HBM) \pm 8kV
 - 3000Vrms/5000Vrms for 1 minute per UL 1577
- CSA Component Acceptance Notice 5A
 - DIN VDE V 0884-11:2017-01
 - $V_{IORM} = 565V$ peak/1200V peak
 - CQC certification per GB4943.1-2011
- 3 V to 5.5 V level translation
- AEC-Q100 qualification
- Wide temperature range: $-40^{\circ}C$ to $125^{\circ}C$
- RoHS-compliant, NB SOIC-16, WB SOIC-16 and SSOP16 package

APPLICATIONS

- General-purpose multichannel isolation
- Industrial field bus isolation
- Isolation Industrial automation systems
- Isolated switch mode supplies
- Isolated ADC, DAC
- Motor control

FUNCTIONAL BLOCK DIAGRAMS

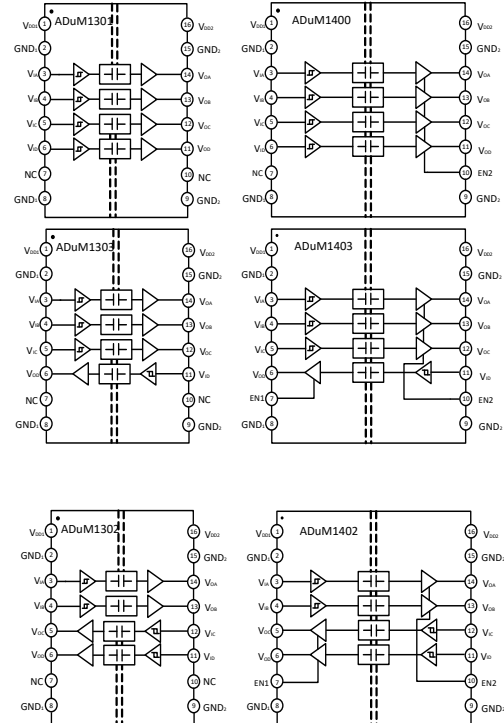


Figure 1. ADuM130x/140x functional Block Diagram

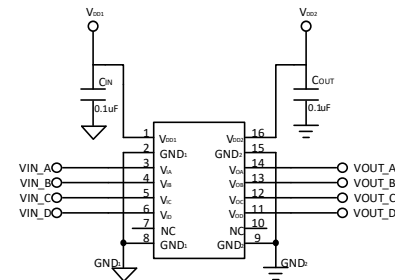


Figure 2. ADuM1301 Typical Application Circuit

PIN CONFIGURATIONS AND FUNCTIONS

Table 1. ADuM1301/1401 Pin Function Descriptions

| Pin No. | Name | Description |
|---------|------------------|---|
| 1 | V _{DD1} | Supply Voltage for Isolator Side 1. |
| 2 | GND ₁ | Ground 1. This pin is the ground reference for Isolator Side 1. |
| 3 | V _{IA} | Logic Input A. |
| 4 | V _{IB} | Logic Input B. |
| 5 | V _{IC} | Logic Input C. |
| 6 | V _{ID} | Logic Input D. |
| 7 | NC | No connect. |
| 8 | GND ₁ | Ground 1. This pin is the ground reference for Isolator Side 1. |
| 9 | GND ₂ | Ground 2. This pin is the ground reference for Isolator Side 2. |
| 10 | NC /EN2 | No connect for ADuM1301. |
| | | Output enable for ADuM1401. Output pins on side 2 are enabled when EN2 is high or open and in high-impedance state when EN2 is low. |
| 11 | V _{OD} | Logic Output D. |
| 12 | V _{OC} | Logic Output C. |
| 13 | V _{OB} | Logic Output B. |
| 14 | V _{OA} | Logic Output A. |
| 15 | GND ₂ | Ground 2. This pin is the ground reference for Isolator Side 2. |
| 16 | V _{DD2} | Supply Voltage for Isolator Side 2. |

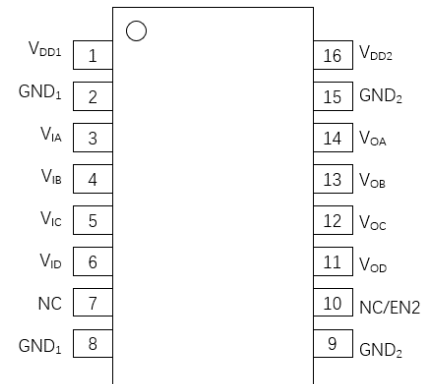


Figure 3. ADuM1301/1401 Pin Configuration

Table 2. ADuM1303/1403 Pin Function Descriptions

| Pin No. | Name | Description |
|---------|------------------|---|
| 1 | V _{DD1} | Supply Voltage for Isolator Side 1. |
| 2 | GND ₁ | Ground 1. This pin is the ground reference for Isolator Side 1. |
| 3 | V _{IA} | Logic Input A. |
| 4 | V _{IB} | Logic Input B. |
| 5 | V _{IC} | Logic Input C. |
| 6 | V _{OD} | Logic Output D. |
| 7 | NC/EN1 | No connect for ADuM1303. |
| | | Output enable 1 for ADuM1403. Output pins on side 1 are enabled when EN1 is high or open and in high-impedance state when EN1 is low. |
| 8 | GND ₁ | Ground 1. This pin is the ground reference for Isolator Side 1. |
| 9 | GND ₂ | Ground 2. This pin is the ground reference for Isolator Side 2. |
| 10 | NC/EN2 | No connect for ADuM1403. |
| | | Output enable 2 for ADuM1403. Output pins on side 2 are enabled when EN2 is high or open and in high-impedance state when EN2 is low. |
| 11 | V _{ID} | Logic Input D. |
| 12 | V _{OC} | Logic Output C. |
| 13 | V _{OB} | Logic Output B. |
| 14 | V _{OA} | Logic Output A. |
| 15 | GND ₂ | Ground 2. This pin is the ground reference for Isolator Side 2. |
| 16 | V _{DD2} | Supply Voltage for Isolator Side 2. |

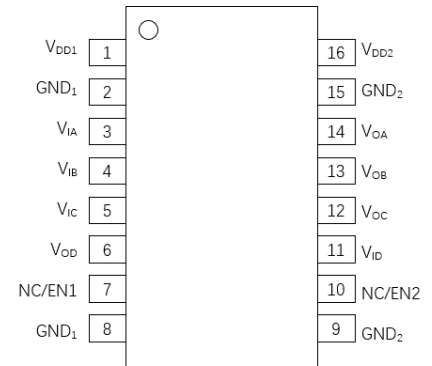


Figure 4. ADuM1303/1403 Pin Configuration

Table 3. ADuM1302/1402 Pin Function Descriptions

| Pin No. | Name | Description |
|---------|------------------|---|
| 1 | V _{DD1} | Supply Voltage for Isolator Side 1. |
| 2 | GND ₁ | Ground 1. This pin is the ground reference for Isolator Side 1. |
| 3 | V _{IA} | Logic Input A. |
| 4 | V _{IB} | Logic Input B. |
| 5 | V _{OC} | Logic Output C. |
| 6 | V _{OD} | Logic Output D. |
| 7 | NC/EN1 | No connect for ADuM1302. |
| | | Output enable 1 for ADuM1402. Output pins on side 1 are enabled when EN1 is high or open and in high-impedance state when EN1 is low. |
| 8 | GND ₁ | Ground 1. This pin is the ground reference for Isolator Side 1. |
| 9 | GND ₂ | Ground 2. This pin is the ground reference for Isolator Side 2. |
| 10 | NC/EN2 | No connect for ADuM1302. |
| | | Output enable 2 for ADuM1402. Output pins on side 2 are enabled when EN2 is high or open and in high-impedance state when EN2 is low. |
| 11 | V _{ID} | Logic Input D. |
| 12 | V _{IC} | Logic Input C. |
| 13 | V _{OB} | Logic Output B. |
| 14 | V _{OA} | Logic Output A. |
| 15 | GND ₂ | Ground 2. This pin is the ground reference for Isolator Side 2. |
| 16 | V _{DD2} | Supply Voltage for Isolator Side 2. |

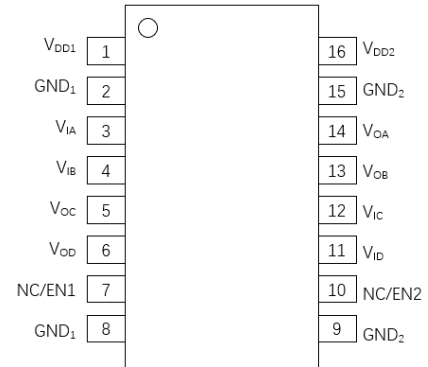


Figure 5. ADuM1302/1402 Pin Configuration

ABSOLUTE MAXIMUM RATINGS

TA = 25°C, unless otherwise noted.

Table 4. Absolute Maximum Ratings⁴

| Parameter | Rating |
|--|-----------------------------------|
| Supply Voltages (V _{DD1} -GND ₁ , V _{DD2} -GND ₂) | -0.5 V ~ +7.0 V |
| Input Voltages (V _{IA} , V _{IB}) ¹ | -0.5 V ~ V _{DDx} + 0.5 V |
| Output Voltages (V _{OA} , V _{OB}) ¹ | -0.5 V ~ V _{DDx} + 0.5 V |
| Average Output Current per Pin ² Side 1 Output Current (I _{O1}) | -10 mA ~ +10 mA |
| Average Output Current per Pin ² Side 2 Output Current (I _{O2}) | -10 mA ~ +10 mA |
| Common-Mode Transients Immunity ³ | -200 kV/μs ~ +200 kV/μs |
| Storage Temperature (T _{ST}) Range | -65°C ~ +150°C |
| Ambient Operating Temperature (T _A) Range | -40°C ~ +125°C |

Notes:

¹ V_{DDx} is the side voltage power supply V_{DD}, where x = 1 or 2.

² See Figure 6 for the maximum rated current values for various temperatures.

³ See Figure 18 for Common-mode transient immunity (CMTI) measurement.

⁴ Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

RECOMMENDED OPERATING CONDITIONS

Table 5. Recommended Operating Conditions

| Parameter | Symbol | Min | Typ | Max | Unit |
|---------------------------------|-------------------------------|-----------------------------------|-----|-------------------------------|------|
| Supply Voltage | V _{DDx} ¹ | 3 | | 5.5 | V |
| High Level Input Signal Voltage | V _{IH} | 0.7*V _{DDx} ¹ | | V _{DDx} ¹ | V |

| Parameter | Symbol | Min | Typ | Max | Unit |
|--------------------------------|----------|-----|-----|-----------------------|------|
| Low Level Input Signal Voltage | V_{IL} | 0 | | $0.3 \cdot V_{DDx}^1$ | V |
| High Level Output Current | I_{OH} | -6 | | | mA |
| Low Level Output Current | I_{OL} | | | 6 | mA |
| Data Rate | | 0 | | 200 | Mbps |
| Junction Temperature | T_J | -40 | | 150 | °C |
| Ambient Operating Temperature | T_A | -40 | | 125 | °C |

Notes:

¹ V_{DDx} is the side voltage power supply V_{DD} , where $x = 1$ or 2 .

Truth Tables

Table 6. ADuM130x/140x Truth Table

| V_{ix} Input ¹ | V_{DDI} State ¹ | V_{DDO} State ¹ | Default Low V_{Ox} Output ¹ | Default High V_{Ox} Output ¹ | Test Conditions /Comments |
|-----------------------------|------------------------------|------------------------------|--|---|-----------------------------|
| Low | Powered ² | Powered ² | Low | Low | Normal operation |
| High | Powered ² | Powered ² | High | High | Normal operation |
| Open | Powered ² | Powered ² | Low | High | Default output |
| Don't Care ⁴ | Unpowered ³ | Powered ² | Low | High | Default output ⁵ |
| Don't Care ⁴ | Powered ² | Unpowered ³ | High Impedance | High Impedance | |

Notes:

¹ V_{ix}/V_{Ox} are the input/output signals of a given channel (A or B). V_{DDI}/V_{DDO} are the supply voltages on the input/output signal sides of this given channel.

² Powered means $V_{DDx} \geq 2.95$ V

³ Unpowered means $V_{DDx} < 2.30$ V

⁴ Input signal (V_{ix}) must be in a low state to avoid powering the given V_{DDI} through its ESD protection circuitry.

⁵ If the V_{DDI} goes into unpowered status, the channel outputs the default logic signal after around 1 μ s. If the V_{DDI} goes into powered status, the channel outputs the input status logic signal after around 3 μ s.

Table 7. ADuM130x/140x Truth Table

| V_{ix} Input ¹ | EN1/2 State | V_{DDI} State ¹ | V_{DDO} State ¹ | Default Low V_{Ox} Output ¹ | Default High V_{Ox} Output ¹ | Test Conditions /Comments |
|-----------------------------|-------------------------|------------------------------|------------------------------|--|---|-----------------------------|
| Low | High or NC | Powered ² | Powered ² | Low | Low | Normal operation |
| High | High or NC | Powered ² | Powered ² | High | High | Normal operation |
| Don't Care ⁴ | L | Powered ² | Powered ² | High Impedance | High Impedance | Disabled |
| Open | High or NC | Powered ² | Powered ² | Low | High | Default output ⁵ |
| Don't Care ⁴ | High or NC | Unpowered ³ | Powered ² | Low | High | Default output ⁵ |
| Don't Care ⁴ | L | Unpowered ³ | Powered ² | High Impedance | High Impedance | |
| Don't Care ⁴ | Don't Care ⁴ | Powered ² | Unpowered ³ | High Impedance | High Impedance | |

Notes:

¹ V_{ix}/V_{Ox} are the input/output signals of a given channel (A or B). V_{DDI}/V_{DDO} are the supply voltages on the input/output signal sides of this given channel.

² Powered means $V_{DDx} \geq 2.95$ V

³ Unpowered means $V_{DDx} < 2.30$ V

⁴ Input signal (V_{ix}) must be in a low state to avoid powering the given V_{DDI} through its ESD protection circuitry.

⁵ If the V_{DDI} goes into unpowered status, the channel outputs the default logic signal after around 1 μ s. If the V_{DDI} goes into powered status, the channel outputs the input status logic signal after around 3 μ s.

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS

Table 8. ADuM130x Switching Specifications

$V_{DD1} - V_{GND1} = V_{DD2} - V_{GND2} = 3.3V_{DC} \pm 10\%$ or $5V_{DC} \pm 10\%$, $T_A = 25^\circ\text{C}$, unless otherwise noted.

| Parameter | Symbol | Min | Typ | Max | Unit | Test Conditions/Comments |
|---------------------|--------|-----|-----|-----|------|---|
| Minimum Pulse Width | PW | | | 5 | ns | Within pulse width distortion (PWD) limit |

| Parameter | Symbol | Min | Typ | Max | Unit | Test Conditions/Comments |
|---|--------------------|-----|---------|------|------------------|--|
| Maximum Data Rate | | 200 | | | Mbps | Within PWD limit |
| Propagation Delay Time ¹ | t_{pHL}, t_{pLH} | 5.5 | 8 | 12.5 | ns | 5V _{DC} supply |
| | | 6.5 | 9 | 13.5 | ns | 3.3V _{DC} supply |
| Pulse Width Distortion | PWD | 0.3 | 3.0 | | ns | The max different time between t_{pHL} and t_{pLH} @ 5V _{DC} supply. And The value is $ t_{pHL} - t_{pLH} $ |
| | | 0.4 | 3.0 | | ns | The max different time between t_{pHL} and t_{pLH} @ 3.3V _{DC} supply. And The value is $ t_{pHL} - t_{pLH} $ |
| Part to Part Propagation Delay Skew | t_{psk} | | | 2 | ns | The max different propagation delay time between any two devices at the same temperature, load and voltage @ 5V _{DC} supply |
| | | | | 2 | ns | The max different propagation delay time between any two devices at the same temperature, load and voltage @ 3.3V _{DC} supply |
| Channel to Channel Propagation Delay Skew | t_{csk} | 0 | 1.8 | | ns | The max amount propagation delay time differs between any two output channels in the single device @ 5V _{DC} supply. |
| | | 0 | 2 | | ns | The max amount propagation delay time differs between any two output channels in the single device @ 3.3V _{DC} supply |
| Output Signal Rise/Fall Time ⁴ | t_r/t_f | | 1.5 | | ns | See Figure 10. |
| Dynamic Input Supply Current per Channel | $I_{DDI(D)}$ | | 9 | | μA /Mbps | Inputs switching, 50% duty cycle square wave, CL = 0 pF @ 5V _{DC} Supply |
| Dynamic Output Supply Current per Channel | $I_{DDO(D)}$ | | 38 | | μA /Mbps | |
| Dynamic Input Supply Current per Channel | $I_{DDI(D)}$ | | 5 | | μA /Mbps | Inputs switching, 50% duty cycle square wave, CL = 0 pF @ 3.3V _{DC} Supply |
| Dynamic Output Supply Current per Channel | $I_{DDO(D)}$ | | 23 | | μA /Mbps | |
| Common-Mode Transient Immunity ³ | CMTI | | 75 | | kV/ μs | $V_{IN} = V_{DDx}^2$ or 0V, $V_{CM} = 1000$ V |
| Jitter | | | 120 | | ps p-p | See the Jitter Measurement section |
| | | | 20 | | ps rms | |
| ESD(HBM - Human body model) | ESD | | ± 8 | | kV | |

Notes:

¹ t_{pLH} = low-to-high propagation delay time, t_{pHL} = high-to-low propagation delay time. See Figure 11.

² V_{DDx} is the side voltage power supply VDD, where x = 1 or 2.

³ See Figure 18 for Common-mode transient immunity (CMTI) measurement.

⁴ t_r means is the time from 10% amplitude to 90% amplitude of the rising edge of the signal, t_f means is the time from 90% amplitude to 10% amplitude of the falling edge of the signal.

Table 9. ADuM140x Switching Specifications

$V_{DD1} - V_{GND1} = V_{DD2} - V_{GND2} = 3.3V_{DC} \pm 10\%$ or $5V_{DC} \pm 10\%$, $T_A = 25^\circ C$, unless otherwise noted.

| Parameter | Symbol | Min | Typ | Max | Unit | Test Conditions/Comments |
|-------------------------------------|--------------------|-----|-----|------|------|--|
| Minimum Pulse Width | PW | | | 5 | ns | Within pulse width distortion (PWD) limit |
| Maximum Data Rate | | 200 | | | Mbps | Within PWD limit |
| Propagation Delay Time ¹ | t_{pHL}, t_{pLH} | | 12 | 16 | ns | 5V _{DC} supply |
| | | | 14 | 18.5 | ns | 3.3V _{DC} supply |
| Pulse Width Distortion | PWD | | 0.3 | 3.0 | ns | The max different time between t_{pHL} and t_{pLH} @ 5V _{DC} supply. And The value is $ t_{pHL} - t_{pLH} $ |

| Parameter | Symbol | Min | Typ | Max | Unit | Test Conditions/Comments |
|---|--------------|-----|-----|-----|----------|--|
| | | | 0.4 | 3.0 | ns | The max different time between t_{pHL} and t_{pLH} @ 3.3V _{DC} supply. And The value is $ t_{pHL} - t_{pLH} $ |
| Part to Part Propagation Delay Skew | t_{psk} | | | 2 | ns | The max different propagation delay time between any two devices at the same temperature, load and voltage @ 5V _{DC} supply |
| | | | | 2 | ns | The max different propagation delay time between any two devices at the same temperature, load and voltage @ 3.3V _{DC} supply |
| Channel to Channel Propagation Delay Skew | t_{csk} | | 0 | 1.8 | ns | The max amount propagation delay time differs between any two output channels in the single device @ 5V _{DC} supply. |
| | | | 0 | 2 | ns | The max amount propagation delay time differs between any two output channels in the single device @ 3.3V _{DC} supply |
| Output Signal Rise/Fall Time ⁴ | t_r/t_f | | 1.5 | | ns | See Figure 10. |
| Disable propagation delay, high-to-high impedance output ⁵ | t_{PHZ} | | 20 | 41 | ns | @ 5V _{DC} supply |
| | | | 24 | 50 | ns | @ 3.3V _{DC} supply |
| Disable propagation delay, low-to-high impedance output | t_{PLZ} | | 20 | 41 | ns | @ 5V _{DC} supply |
| | | | 24 | 50 | ns | @ 3.3V _{DC} supply |
| Enable propagation delay, high impedance-to-high output | t_{PZH} | | 12 | 25 | ns | @ 5V _{DC} supply, for ADuM1400 |
| | | | 16 | 33 | ns | @ 3.3V _{DC} supply, for ADuM1400 |
| | | | 1.7 | 5.7 | us | @ 5V _{DC} supply, for ADuM1401 |
| | | | 1.1 | 4.4 | us | @ 3.3V _{DC} supply, for ADuM1401 |
| Enable propagation delay, high impedance-to-low output | t_{PZL} | | 1.7 | 5.7 | us | @ 5V _{DC} supply, for ADuM1400 |
| | | | 1.1 | 4.4 | us | @ 3.3V _{DC} supply, for ADuM1400 |
| | | | 12 | 25 | ns | @ 5V _{DC} supply, for ADuM1401 |
| | | | 16 | 33 | ns | @ 3.3V _{DC} supply, for ADuM1401 |
| Dynamic Input Supply Current per Channel | $I_{DDI(D)}$ | | 10 | | μA /Mbps | Inputs switching, 50% duty cycle square wave, CL = 0 pF @ 5V _{DC} Supply |
| Dynamic Output Supply Current per Channel | $I_{DDO(D)}$ | | 45 | | μA /Mbps | |
| Dynamic Input Supply Current per Channel | $I_{DDI(D)}$ | | 9 | | μA /Mbps | Inputs switching, 50% duty cycle square wave, CL = 0 pF @ 3.3V _{DC} Supply |
| Dynamic Output Supply Current per Channel | $I_{DDO(D)}$ | | 28 | | μA /Mbps | |
| Common-Mode Transient Immunity ³ | CMTI | | 120 | | kV/μs | $V_{IN} = V_{DDx}^2$ or 0V, $V_{CM} = 1000$ V |
| Jitter | | | 180 | | ps p-p | See the Jitter Measurement section |
| | | | 30 | | ps rms | |
| ESD (HBM - Human body model) | ESD | | ±8 | | kV | |

Notes:

¹ t_{pLH} = low-to-high propagation delay time, t_{pHL} = high-to-low propagation delay time. See Figure 11.

² V_{DDx} is the side voltage power supply VDD, where x = 1 or 2.

³See Figure 18 for Common-mode transient immunity (CMTI) measurement.

⁴ t_r means is the time from 10% amplitude to 90% amplitude of the rising edge of the signal, t_f means is the time from 90% amplitude to 10% amplitude of the falling edge of the signal.

⁵See Figure 12, Figure 13 for t_{PLZ} , t_{PZL} measurement, see Figure 14, Figure 15 for t_{PHZ} , t_{PZH} measurement.

Table 10. DC Specifications

 $V_{DD1} - V_{GND1} = V_{DD2} - V_{GND2} = 3.3V_{DC} \pm 10\%$ or $5V_{DC} \pm 10\%$, $T_A = 25^\circ C$, unless otherwise noted.

| | Symbol | Min | Typ | Max | Unit | Test Conditions/Comments |
|--|--------------|-------------------|-------------------|-------------------|---------|---|
| Rising Input Signal Voltage Threshold | V_{IT+} | | $0.6 * V_{DDx}^1$ | $0.7 * V_{DDx}^1$ | V | |
| Falling Input Signal Voltage Threshold | V_{IT-} | $0.3 * V_{DDx}^1$ | $0.4 * V_{DDx}^1$ | | V | |
| High Level Output Voltage | V_{OH}^1 | $V_{DDx} - 0.1$ | V_{DDx} | | V | -20 μA output current |
| | | $V_{DDx} - 0.2$ | $V_{DDx} - 0.1$ | | V | -2 mA output current |
| Low Level Output Voltage | V_{OL} | | 0 | 0.1 | V | 20 μA output current |
| | | | 0.1 | 0.2 | V | 2 mA output current |
| Input Current per Signal Channel | I_{IN} | -10 | 0.5 | 10 | μA | $0 V \leq \text{Signal voltage} \leq V_{DDx}^1$ |
| V_{DDx}^1 Undervoltage Rising Threshold | V_{DDxUV+} | 2.45 | 2.75 | 2.95 | V | |
| V_{DDx}^1 Undervoltage Falling Threshold | V_{DDxUV-} | 2.30 | 2.60 | 2.75 | V | |
| V_{DDx}^1 Hysteresis | V_{DDxUVH} | | 0.15 | | V | |

Notes:

¹ V_{DDx} is the side voltage power supply V_{DD} , where x = 1 or 2.

Table 11. Quiescent Supply Current

 $V_{DD1} - V_{GND1} = V_{DD2} - V_{GND2} = 3.3V_{DC} \pm 10\%$ or $5V_{DC} \pm 10\%$, $T_A = 25^\circ C$, $C_L = 0$ pF, unless otherwise noted.

| Part | Symbol | Min | Typ | Max | Unit | Test Conditions | | |
|----------|--------------|------|------|------|------|--------------------|---------------------------|-----------------------------|
| | | | | | | Supply voltage | Input signal | |
| ADuM1301 | $I_{DD1(Q)}$ | 0.13 | 0.16 | 0.21 | mA | 5V _{DC} | $V_I = 0V$ for 130x/140x0 | |
| | $I_{DD2(Q)}$ | 1.56 | 1.95 | 2.54 | | | $V_I = 5V$ for 130x/140x1 | |
| | $I_{DD1(Q)}$ | 0.32 | 0.39 | 0.51 | mA | | 3.3V _{DC} | $V_I = 5V$ for 130x/140x0 |
| | $I_{DD2(Q)}$ | 1.48 | 1.85 | 2.40 | | | | $V_I = 0V$ for 130x/140x1 |
| | $I_{DD1(Q)}$ | 0.13 | 0.16 | 0.21 | mA | 3.3V _{DC} | | $V_I = 0V$ for 130x/140x0 |
| | $I_{DD2(Q)}$ | 1.54 | 1.93 | 2.51 | | | | $V_I = 3.3V$ for 130x/140x1 |
| | $I_{DD1(Q)}$ | 0.23 | 0.29 | 0.38 | mA | | 3.3V _{DC} | $V_I = 3.3V$ for 130x/140x0 |
| | $I_{DD2(Q)}$ | 1.42 | 1.77 | 2.30 | | | | $V_I = 0V$ for 130x/140x1 |
| ADuM1303 | $I_{DD1(Q)}$ | 0.48 | 0.60 | 0.79 | mA | 5V _{DC} | | $V_I = 0V$ for 130x/140x0 |
| | $I_{DD2(Q)}$ | 1.20 | 1.50 | 1.95 | | | | $V_I = 5V$ for 130x/140x1 |
| | $I_{DD1(Q)}$ | 0.59 | 0.74 | 0.97 | mA | | 3.3V _{DC} | $V_I = 5V$ for 130x/140x0 |
| | $I_{DD2(Q)}$ | 1.17 | 1.47 | 1.91 | | | | $V_I = 0V$ for 130x/140x1 |
| | $I_{DD1(Q)}$ | 0.48 | 0.60 | 0.78 | mA | 3.3V _{DC} | | $V_I = 0V$ for 130x/140x0 |
| | $I_{DD2(Q)}$ | 1.19 | 1.48 | 1.93 | | | | $V_I = 3.3V$ for 130x/140x1 |
| | $I_{DD1(Q)}$ | 0.52 | 0.66 | 0.85 | mA | | 3.3V _{DC} | $V_I = 3.3V$ for 130x/140x0 |
| | $I_{DD2(Q)}$ | 1.12 | 1.40 | 1.82 | | | | $V_I = 0V$ for 130x/140x1 |
| ADuM1302 | $I_{DD1(Q)}$ | 0.84 | 1.05 | 1.36 | mA | 5V _{DC} | | $V_I = 0V$ for 130x/140x0 |
| | $I_{DD2(Q)}$ | 0.84 | 1.05 | 1.36 | | | | $V_I = 5V$ for 130x/140x1 |
| | $I_{DD1(Q)}$ | 0.87 | 1.09 | 1.42 | mA | | 3.3V _{DC} | $V_I = 5V$ for 130x/140x0 |
| | $I_{DD2(Q)}$ | 0.87 | 1.09 | 1.42 | | | | $V_I = 0V$ for 130x/140x1 |
| | $I_{DD1(Q)}$ | 0.83 | 1.04 | 1.35 | mA | 3.3V _{DC} | | $V_I = 0V$ for 130x/140x0 |
| | $I_{DD2(Q)}$ | 0.83 | 1.04 | 1.35 | | | | $V_I = 3.3V$ for 130x/140x1 |
| | $I_{DD1(Q)}$ | 0.82 | 1.02 | 1.33 | mA | | 3.3V _{DC} | $V_I = 3.3V$ for 130x/140x0 |
| | $I_{DD2(Q)}$ | 0.82 | 1.02 | 1.33 | | | | $V_I = 0V$ for 130x/140x1 |
| ADuM1401 | $I_{DD1(Q)}$ | 0.11 | 0.13 | 0.21 | mA | 5V _{DC} | | $V_I = 0V$ for 130x/140x0 |
| | $I_{DD2(Q)}$ | 1.56 | 2.18 | 2.93 | | | | $V_I = 5V$ for 130x/140x1 |
| | $I_{DD1(Q)}$ | 0.32 | 0.56 | 0.79 | mA | | 3.3V _{DC} | $V_I = 5V$ for 130x/140x0 |
| | $I_{DD2(Q)}$ | 1.48 | 2.00 | 2.72 | | | | $V_I = 0V$ for 130x/140x1 |
| | $I_{DD1(Q)}$ | 0.10 | 0.12 | 0.21 | mA | 3.3V _{DC} | | $V_I = 0V$ for 130x/140x0 |
| | $I_{DD2(Q)}$ | 1.54 | 2.11 | 2.85 | | | | $V_I = 3.3V$ for 130x/140x1 |

| Part | Symbol | Min | Typ | Max | Unit | Test Conditions | | |
|----------------------|----------------------|----------------------|------|------|------|----------------------|------------------------|----------------------|
| | | | | | | Supply voltage | Input signal | |
| | I _{DD1} (Q) | 0.23 | 0.35 | 0.49 | mA | | VI=3.3V for 130x/140x0 | |
| | I _{DD2} (Q) | 1.42 | 1.94 | 2.62 | mA | | VI=0V for 130x/140x1 | |
| ADuM1403 | I _{DD1} (Q) | 0.50 | 0.63 | 0.82 | mA | 5V _{DC} | VI=0V for 130x/140x0 | |
| | I _{DD2} (Q) | 1.28 | 1.60 | 2.07 | mA | | VI=5V for 130x/140x1 | |
| | I _{DD1} (Q) | 0.75 | 0.94 | 1.22 | mA | | VI=5V for 130x/140x0 | |
| | I _{DD2} (Q) | 1.17 | 1.47 | 1.91 | mA | VI=0V for 130x/140x1 | | |
| | I _{DD1} (Q) | 0.48 | 0.60 | 0.78 | mA | 3.3V _{DC} | VI=0V for 130x/140x0 | |
| | I _{DD2} (Q) | 1.24 | 1.55 | 2.01 | mA | | VI=3.3V for 130x/140x1 | |
| ADuM1402 | I _{DD1} (Q) | 0.61 | 0.77 | 1.00 | mA | 5V _{DC} | VI=3.3V for 130x/140x0 | |
| | I _{DD2} (Q) | 1.13 | 1.42 | 1.84 | mA | | VI=0V for 130x/140x1 | |
| | I _{DD1} (Q) | 0.89 | 1.12 | 1.46 | mA | | VI=0V for 130x/140x0 | |
| | I _{DD2} (Q) | 0.89 | 1.12 | 1.46 | mA | VI=5V for 130x/140x1 | | |
| | I _{DD1} (Q) | 1.00 | 1.25 | 1.63 | mA | 3.3V _{DC} | VI=5V for 130x/140x0 | |
| | I _{DD2} (Q) | 1.00 | 1.25 | 1.63 | mA | | VI=0V for 130x/140x1 | |
| ADuM1403 | I _{DD1} (Q) | 0.86 | 1.08 | 1.41 | mA | 5V _{DC} | VI=0V for 130x/140x0 | |
| | I _{DD2} (Q) | 0.86 | 1.08 | 1.41 | mA | | VI=3.3V for 130x/140x1 | |
| | I _{DD1} (Q) | 0.89 | 1.12 | 1.45 | mA | | VI=3.3V for 130x.140x0 | |
| | I _{DD2} (Q) | 0.89 | 1.12 | 1.45 | mA | VI=0V for 130x/140x1 | | |
| | ADuM1402 | I _{DD1} (Q) | 0.89 | 1.12 | 1.45 | mA | 5V _{DC} | VI=0V for 130x/140x0 |
| | | I _{DD2} (Q) | 0.89 | 1.12 | 1.45 | mA | | VI=5V for 130x/140x1 |
| I _{DD1} (Q) | | 1.00 | 1.25 | 1.63 | mA | VI=0V for 130x/140x1 | | |
| I _{DD2} (Q) | | 1.00 | 1.25 | 1.63 | mA | VI=5V for 130x/140x0 | | |
| I _{DD1} (Q) | | 0.86 | 1.08 | 1.41 | mA | 3.3V _{DC} | VI=3.3V for 130x/140x1 | |
| I _{DD2} (Q) | | 0.86 | 1.08 | 1.41 | mA | | VI=0V for 130x/140x0 | |

Table 12.Total Supply Current vs. Data Throughput (CL = 0 pF)

V_{DD1} - V_{GND1} = V_{DD2} - V_{GND2} = 3.3V_{DC}±10% or 5V_{DC}±10%, T_A=25°C, C_L = 0 pF, unless otherwise noted.

| Part | Symbol | 2 Mbps | | | 20 Mbps | | | 200 Mbps | | | Unit | Supply voltage |
|----------|------------------|--------|------|-----|---------|------|-----|----------|-------|-----|------|--------------------|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | | |
| ADuM1301 | I _{DD1} | 0.45 | 0.72 | | 0.96 | 1.54 | | 7.44 | 11.90 | | mA | 5V _{DC} |
| | I _{DD2} | 2.24 | 3.59 | | 5.28 | 8.45 | | 34.40 | 55.04 | | | |
| | I _{DD1} | 0.31 | 0.50 | | 0.72 | 1.15 | | 4.32 | 6.91 | | mA | 3.3V _{DC} |
| | I _{DD2} | 2.13 | 3.41 | | 4.29 | 6.86 | | 22.28 | 35.65 | | | |
| ADuM1303 | I _{DD1} | 0.80 | 1.28 | | 1.94 | 3.10 | | 14.12 | 22.59 | | mA | 5V _{DC} |
| | I _{DD2} | 1.76 | 2.82 | | 4.23 | 6.77 | | 27.60 | 44.16 | | | |
| | I _{DD1} | 0.73 | 1.16 | | 1.47 | 2.36 | | 8.74 | 13.98 | | mA | 3.3V _{DC} |
| | I _{DD2} | 1.66 | 2.66 | | 3.41 | 5.46 | | 17.72 | 28.35 | | | |
| ADuM1302 | I _{DD1} | 1.29 | 2.06 | | 2.91 | 4.66 | | 20.80 | 33.28 | | mA | 5V _{DC} |
| | I _{DD2} | 1.29 | 2.06 | | 2.91 | 4.66 | | 20.80 | 33.28 | | | |
| | I _{DD1} | 1.20 | 1.92 | | 2.31 | 3.70 | | 13.16 | 21.06 | | mA | 3.3V _{DC} |
| | I _{DD2} | 1.20 | 1.92 | | 2.31 | 3.70 | | 13.16 | 21.06 | | | |
| ADuM1401 | I _{DD1} | 0.59 | 0.94 | | 2.00 | 3.20 | | 17.40 | 27.84 | | mA | 5V _{DC} |
| | I _{DD2} | 2.49 | 3.98 | | 5.75 | 9.19 | | 38.94 | 62.30 | | | |
| | I _{DD1} | 0.35 | 0.56 | | 1.22 | 1.95 | | 10.16 | 16.26 | | mA | 3.3V _{DC} |
| | I _{DD2} | 2.34 | 3.75 | | 4.68 | 7.49 | | 26.40 | 42.24 | | | |
| ADuM1403 | I _{DD1} | 0.96 | 1.53 | | 2.85 | 4.56 | | 23.62 | 37.79 | | mA | 5V _{DC} |
| | I _{DD2} | 1.90 | 3.04 | | 4.70 | 7.51 | | 31.54 | 50.46 | | | |
| | I _{DD1} | 0.80 | 1.28 | | 2.02 | 3.22 | | 14.46 | 23.14 | | mA | 3.3V _{DC} |
| | I _{DD2} | 1.77 | 2.83 | | 3.80 | 6.08 | | 21.12 | 33.79 | | | |
| ADuM1402 | I _{DD1} | 1.47 | 2.34 | | 3.69 | 5.90 | | 29.68 | 47.49 | | mA | 5V _{DC} |

| Part | Symbol | 2 Mbps | | | 20 Mbps | | | 200 Mbps | | | Unit | Supply voltage |
|------|------------------|--------|------|------|---------|------|------|----------|-------|-------|------|--------------------|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | | |
| | I _{DD2} | | 1.47 | 2.34 | | 3.69 | 5.90 | | 29.68 | 47.49 | | |
| | I _{DD1} | | 1.31 | 2.10 | | 2.85 | 4.56 | | 19.62 | 31.39 | mA | 3.3V _{DC} |
| | I _{DD2} | | 1.31 | 2.10 | | 2.85 | 4.56 | | 19.62 | 31.39 | | |

INSULATION AND SAFETY RELATED SPECIFICATIONS

Table 13. Insulation Specifications

| Parameter | Symbol | Value | | Unit | Test Conditions/Comments |
|--|---------|----------|----------|-------|--|
| | | ADuM130x | ADuM140x | | |
| Rated Dielectric Insulation Voltage | | 3000 | 5000 | V rms | 1-minute duration |
| Minimum External Air Gap (Clearance) | L (CLR) | ≥4 | ≥8 | mm | Measured from input terminals to output terminals, shortest distance through air |
| Minimum External Tracking (Creepage) | L (CRP) | ≥4 | ≥8 | mm | Measured from input terminals to output terminals, shortest distance path along body |
| Minimum Internal Gap (Internal Clearance) | | ≥11 | ≥21 | μm | Insulation distance through insulation |
| Tracking Resistance (Comparative Tracking Index) | CTI | >400 | >400 | V | DIN EN 60112 (VDE 0303-11):2010-05 |
| Material Group | | II | II | | IEC 60112:2003 + A1:2009 |

PACKAGE CHARACTERISTICS

Table 14. Package Characteristics

| Parameter | Symbol | Typical Value | | Unit | Test Conditions/Comments |
|--|-----------------|------------------|------------------|------|---|
| | | ADuM130x | ADuM140x | | |
| Resistance (Input to Output) ¹ | R _{IO} | 10 ¹¹ | 10 ¹¹ | Ω | |
| Capacitance (Input to Output) ¹ | C _{IO} | 1.5 | 1.5 | pF | @1MHz |
| Input Capacitance ² | C _I | 3 | 3 | pF | @1MHz |
| IC Junction to Ambient Thermal Resistance | θ _{JA} | 100 | 45 | °C/W | Thermocouple located at center of package underside |

Notes:

¹The device is considered a 2-terminal device; Short-circuit all terminals on the VDD1 side as one terminal, and short-circuit all terminals on the VDD2 side as the other terminal.

²Testing from the input signal pin to ground.

DIN V VDE V 0884-11 (VDE V 0884-11) INSULATION CHARACTERISTICS

Table 16.VDE Insulation Characteristics

| Description | Test Conditions/Comments | Symbol | Characteristic | | Unit |
|--|---|-------------|---------------------------------|---------------------------------|--------------|
| | | | ADuM130x | ADuM140x | |
| Installation Classification per DIN VDE 0110 For Rated Mains Voltage ≤ 150 V rms For Rated Mains Voltage ≤ 300 V rms For Rated Mains Voltage ≤ 400 V rms | | | I to IV I to III I to III | I to IV I to III I to III | |
| Climatic Classification | | | 40/105/21 | 40/105/21 | |
| Pollution Degree per DIN VDE 0110, Table 1 | | | 2 | 2 | |
| Maximum repetitive peak isolation voltage | | V_{IORM} | 565 | 1200 | V peak |
| Input to Output Test Voltage, Method B1 | $V_{IORM} \times 1.5 = V_{pd(m)}$, 100% production test, $t_{ini} = t_m = 1$ sec, partial discharge < 5 pC | $V_{pd(m)}$ | 848 | 1800 | V peak |
| Input to Output Test Voltage, Method A After Environmental Tests Subgroup 1 After Input and/or Safety Test Subgroup 2 and Subgroup 3 | $V_{IORM} \times 1.3 = V_{pd(m)}$, $t_{ini} = 60$ sec, $t_m = 10$ sec, partial discharge < 5 pC | $V_{pd(m)}$ | 735 | 1560 | V peak |
| | $V_{IORM} \times 1.2 = V_{pd(m)}$, $t_{ini} = 60$ sec, $t_m = 10$ sec, partial discharge < 5 pC | $V_{pd(m)}$ | 678 | 1440 | V peak |
| Highest Allowable Overvoltage | | V_{IOTM} | 4200 | 7071 | V peak |
| Surge Isolation Voltage Basic | Basic insulation, 1.2/50 μ s combination wave, $V_{TEST} = 1.3 \times V_{IOSM}$ (qualification) | V_{IOSM} | 3615 | 5000 | V peak |
| Safety Limiting Values | Maximum value allowed in the event of a failure (see Figure 6) | | | | |
| Maximum Safety Temperature | | T_S | 150 | 150 | $^{\circ}$ C |
| Maximum Power Dissipation at 25 $^{\circ}$ C | | P_S | 1.67 | 2.78 | W |
| Insulation Resistance at T_S | $V_{IO} = 500$ V | R_S | $>10^9$ | $>10^9$ | Ω |

Typical Thermal Characteristic

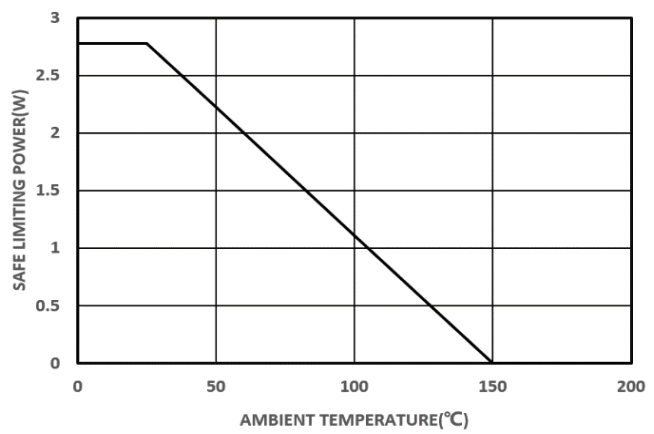
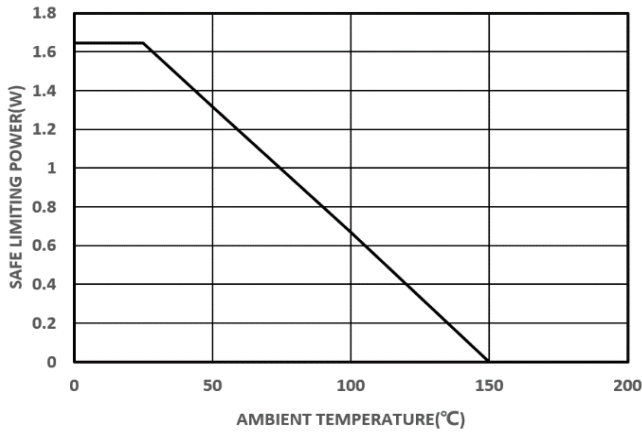


Figure 6. Thermal Derating Curve, Dependence of Safety Limiting Values with Ambient Temperature per VDE (left: ADuM130x; right: ADuM140x)

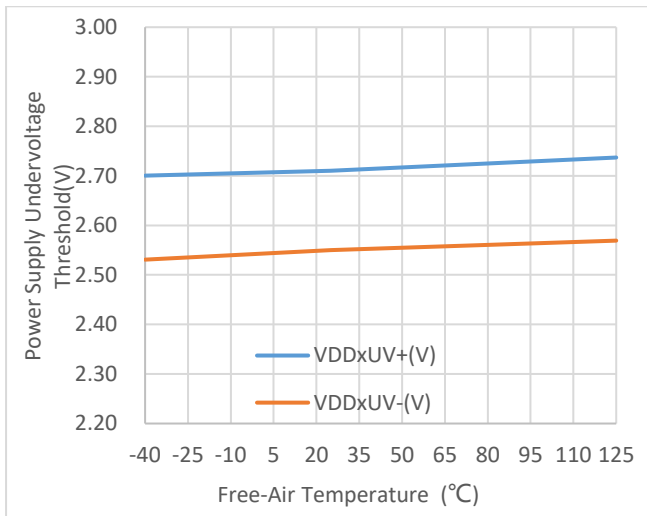


Figure 7. UVLO vs. Free-Air Temperature

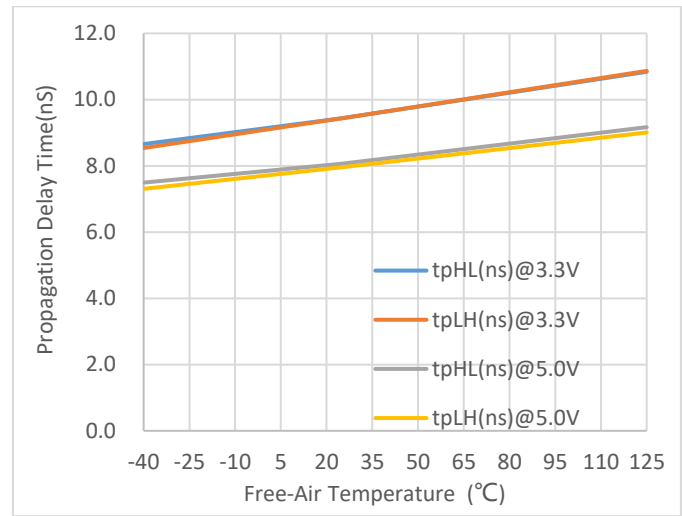


Figure 8. ADuM130x Propagation Delay Time vs. Free-Air Temperature

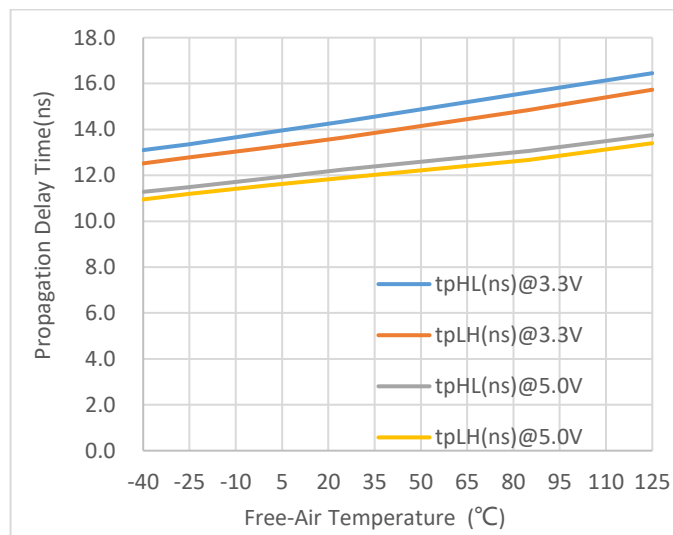


Figure 9. ADuM140x Propagation Delay Time vs. Free-Air Temperature

Timing test information

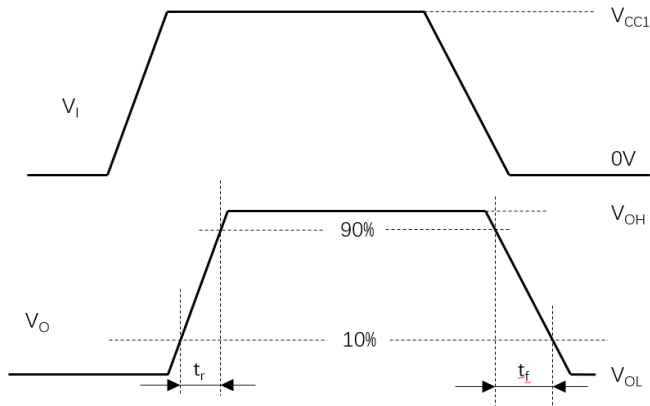


Figure 10. Transition time waveform measurement

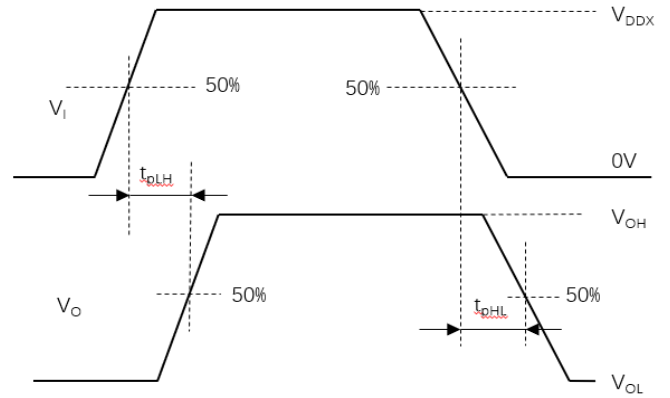


Figure 11. Propagation delay time waveform measurement

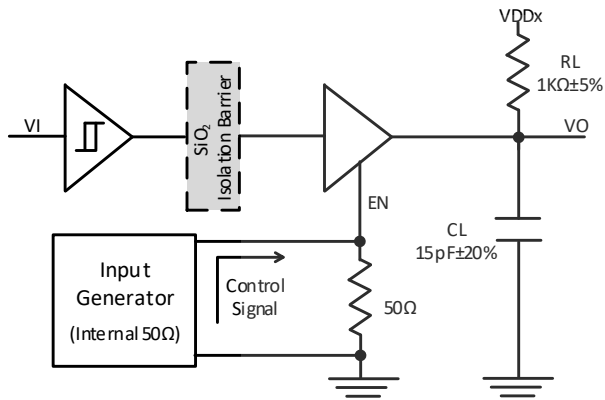


Figure 12. t_{pZL}/t_{pLZ} test circuit

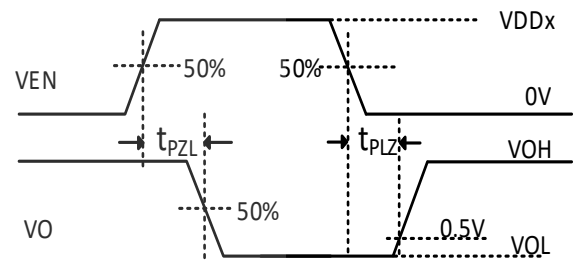


Figure 13. t_{pZL}/t_{pLZ} measurement waveform

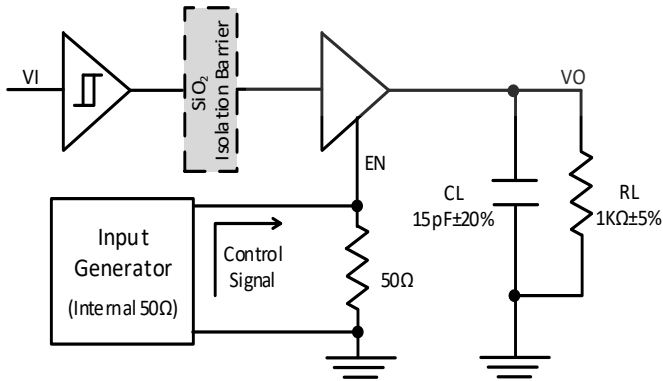


Figure 14. t_{pZH}/t_{pHZ} test circuit

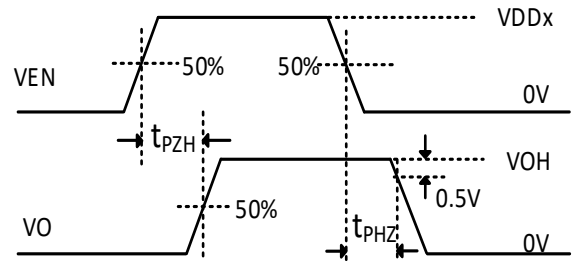


Figure 15. t_{pZH}/t_{pHZ} measurement waveform

PCB LAYOUT

The low-ESR ceramic bypass capacitors must be connected between V_{DD1} and GND_1 and between V_{DD2} and GND_2 . The bypass capacitors are placed on the PCB as close to the isolator device as possible. The recommended bypass capacitor value is between 0.1 μ F and 10 μ F. The user may also include resistors (50–300 Ω) in series with the inputs and outputs if the system is excessively noisy, or in order to enhance the anti ESD ability of the system.

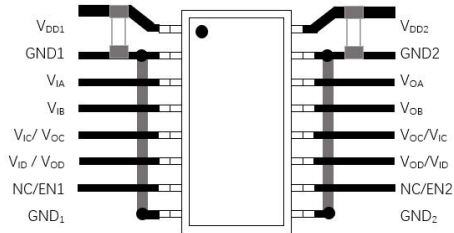


Figure 16. Recommended Printed Circuit Board Layout

Avoid reducing the isolation capability, Keep the space underneath the isolator device free from metal such as planes, pads, traces and vias.

To minimize the impedance of the signal return loop, keep the solid ground plane directly underneath the high-speed signal path, the closer the better. The return path will couple between the nearest ground plane to the signal path. Keep suitable trace width for controlled impedance transmission lines interconnect.

To reduce the rise time degradation, keep the length of input/output signal traces as short as possible, and route low inductance loop for the signal path and its return path.

JITTER MEASUREMENT

The eye diagram shown in the figure below provides the jitter measurement result for the 130x/140x. The Keysight 81160A pulse function arbitrary generator works as the data source for the 130x/140x, which generates 100Mbps pseudo random bit sequence

(PRBS). The Keysight DSOS104A digital storage oscilloscope captures the 130x/140x output waveform and recovers the eye diagram with the SDA tools and eye diagram analysis tools. The result shows a typical measurement jitter data.

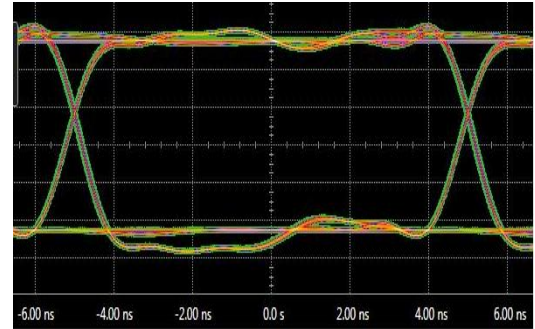


Figure 17. ADuM130x/140x Eye Diagram

CMTI MEASUREMENT

To measure the Common-Mode Transient Immunity (CMTI) of 130x/140x isolator under specified common-mode pulse magnitude (VCM) and specified slew rate of the common-mode pulse (dVCM/dt) and other specified test or ambient conditions, The common-mode pulse generator (G1) will be capable of providing fast rise and fall pulses of specified magnitude and duration of the common-mode pulse (VCM), such that the maximum common-mode slew rates (dVCM/dt) can be applied to 130x/140x isolator coupler under measurement. The common-mode pulse is applied between one side ground GND1 and the other side ground GND2 of 130x/140x isolator, and shall be capable of providing positive transients as well as negative transients.

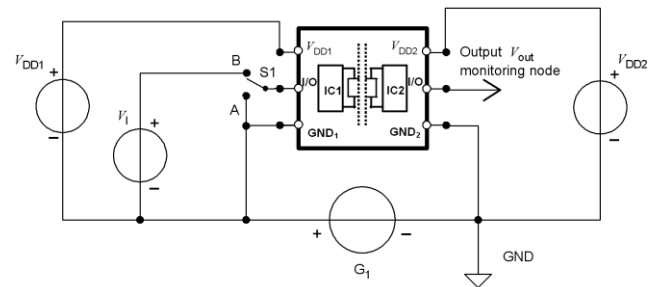


Figure 18. Common-mode transient immunity (CMTI) measurement

OUTLINE DIMENSIONS

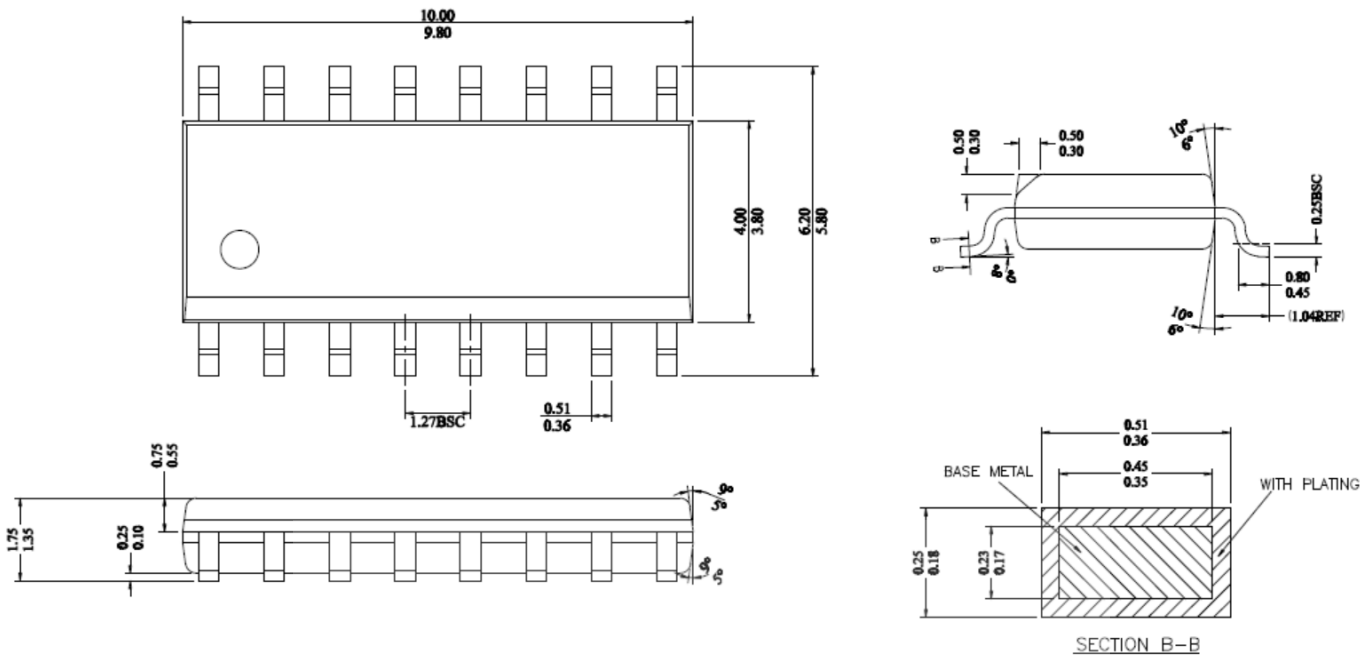


Figure 19.16-Lead Narrow body SOIC Package [NB SOIC-16] –dimension unit(mm)

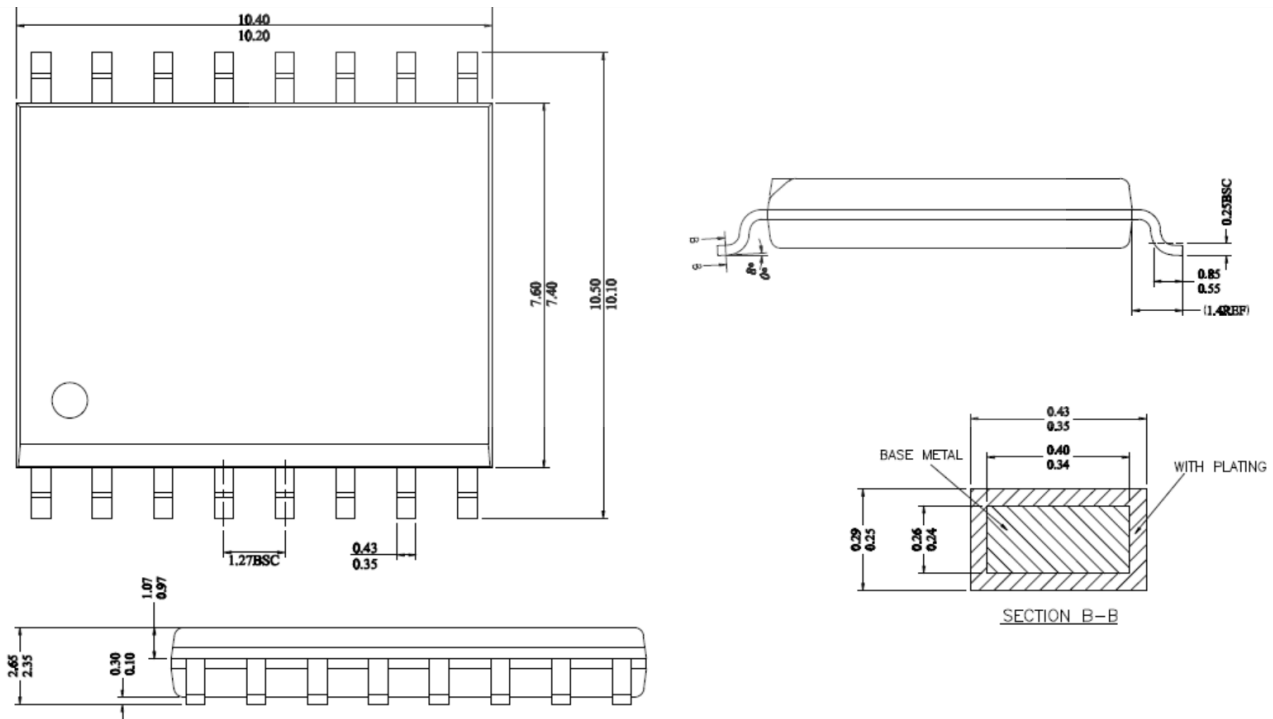
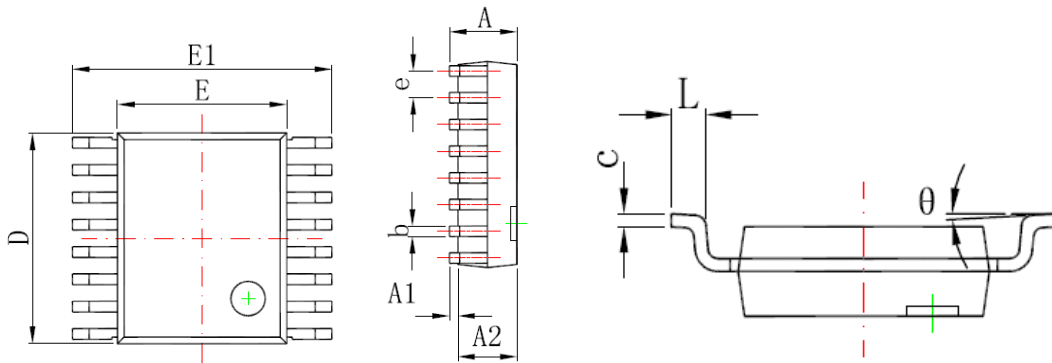


Figure 20.16-Lead Wide Body Outline Package [WB SOIC-16] –dimension unit(mm)



| Symbol | Dimensions In Millimeters | | Dimensions In Inches | |
|----------|---------------------------|-------|----------------------|-------|
| | Min | Max | Min | Max |
| A | 1.350 | 1.750 | 0.053 | 0.069 |
| A1 | 0.100 | 0.250 | 0.004 | 0.010 |
| A2 | 1.350 | 1.550 | 0.053 | 0.061 |
| b | 0.200 | 0.300 | 0.008 | 0.012 |
| c | 0.170 | 0.250 | 0.007 | 0.010 |
| D | 4.700 | 5.100 | 0.185 | 0.200 |
| E | 3.800 | 4.000 | 0.150 | 0.157 |
| E1 | 5.800 | 6.200 | 0.228 | 0.244 |
| e | 0.635(BSC) | | 0.025(BSC) | |
| L | 0.400 | 1.270 | 0.016 | 0.050 |
| θ | 0° | 8° | 0° | 8° |

Figure 21.16-Lead SSOP Outline Package [SSOP-16]

Land Patterns

16-Lead Narrow Body SOIC [NB SOIC-16]

The Figure 22 below illustrates the recommended land pattern details for the 130x/140x in a 16-pin narrow-body SOIC. The table below lists the values for the dimensions shown in the illustration.

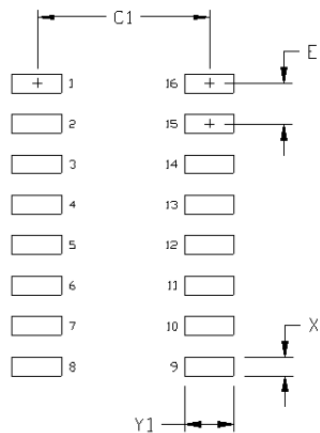


Figure 22.16-Lead Narrow Body SOIC [NB SOIC-16] Land Pattern

Table 17. 16-Lead Narrow Body SOIC [NB SOIC-16] Land Pattern Dimensions

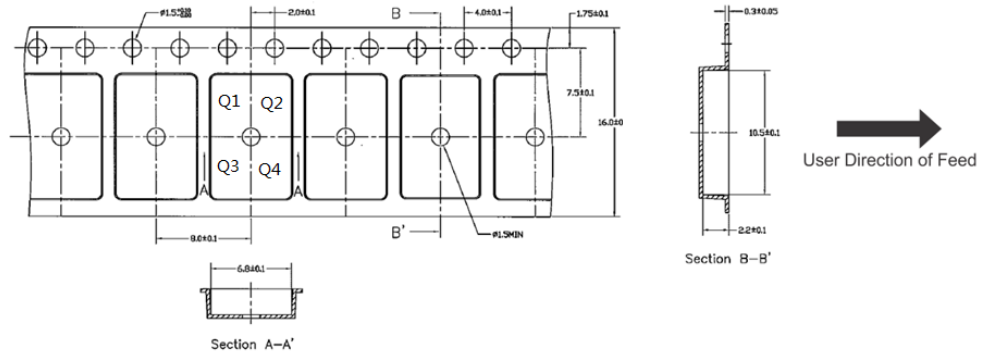
| Dimension | Feature | Parameter | Unit |
|-----------|--------------------|-----------|------|
| C1 | Pad column spacing | 5.40 | mm |
| E | Pad row pitch | 1.27 | mm |
| X1 | Pad width | 0.60 | mm |
| Y1 | Pad length | 1.55 | mm |

Note:

1.This land pattern design is based on IPC -7351

REEL INFORMATION

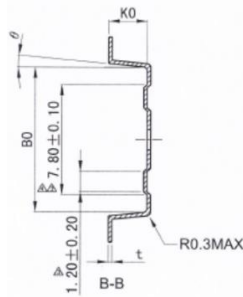
16-Lead Narrow Body SOIC [NB SOIC-16]

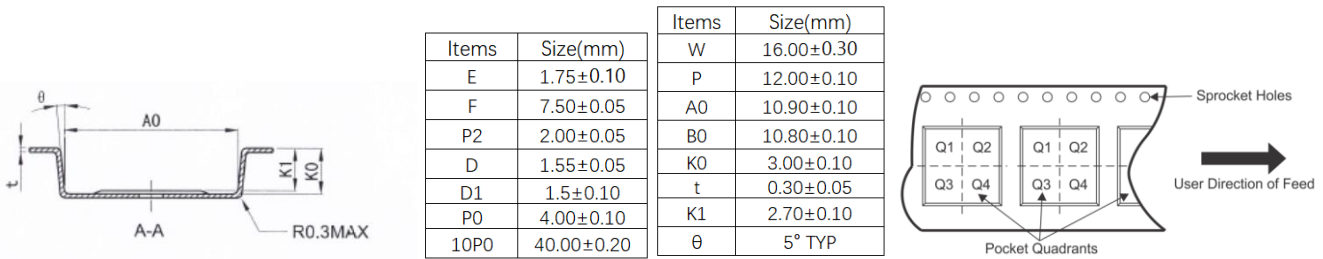


Note: The Pin 1 of the chip is in the quadrant Q1

Figure 23.16-16-Lead Narrow Body SOIC [NB SOIC-16] Reel Information—*dimension unit(mm)*

16-Lead Wide Body SOIC [WB SOIC-16]





Note: The Pin 1of the chip is in the quadrant Q1
 Figure 24.16-Lead Wide Body SOIC [WB SOIC-16] Reel Information

16-Lead SSOP

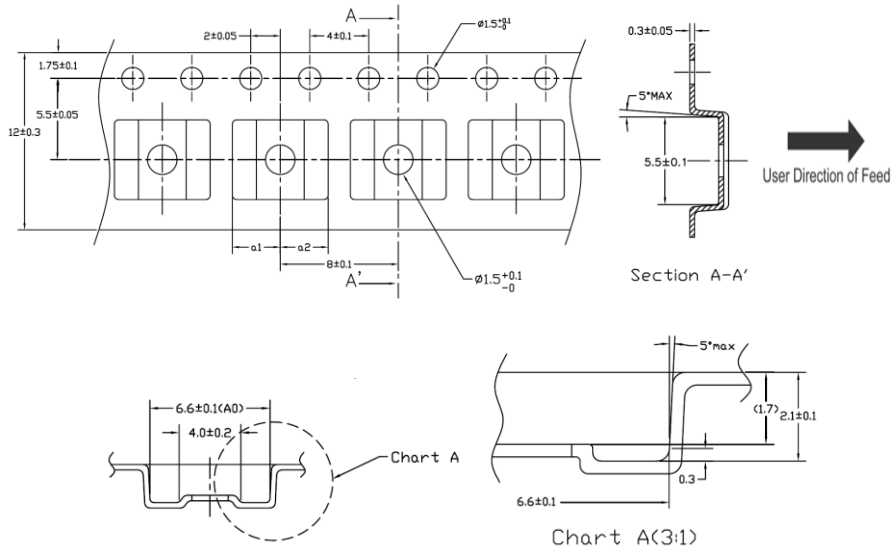


Figure 25. 16-Lead SSOP [SSOP-16] Reel Information—dimension unit(mm)

ORDERING GUIDE

Table 18. Ordering guide

| Model Name | Temperature Range | No. of Inputs, V _{DD1} Side | No. of Inputs, V _{DD2} Side | Withstand Voltage Rating (kV rms) | Fail-Safe Output State | Package | MSL Peak Temp | Quantity per reel |
|------------|-------------------|--------------------------------------|--------------------------------------|-----------------------------------|------------------------|--------------|---------------------|-------------------|
| 1301BRWH | -40 ~125°C | 4 | 0 | 3 | High | NB SOIC-16 | Level-2-260C-1 YEAR | 2500 |
| 1301BRWZ | -40 ~125°C | 4 | 0 | 3 | Low | NB SOIC-16 | Level-2-260C-1 YEAR | 2500 |
| 1303BRWH | -40 ~125°C | 3 | 1 | 3 | High | NB SOIC-16 | Level-2-260C-1 YEAR | 2500 |
| 1303BRWZ | -40 ~125°C | 3 | 1 | 3 | Low | NB SOIC-16 | Level-2-260C-1 YEAR | 2500 |
| 1302BRWH | -40 ~125°C | 2 | 2 | 3 | High | NB SOIC-16 | Level-2-260C-1 YEAR | 2500 |
| 1302BRWZ | -40 ~125°C | 2 | 2 | 3 | Low | NB SOIC-16 | Level-2-260C-1 YEAR | 2500 |
| 1400BRWZ | -40 ~125°C | 4 | 0 | 5 | High | WB SOIC-16 | Level-2-260C-1 YEAR | 1500 |
| 1400BRWQ | -40 ~125°C | 4 | 0 | 5 | High | WB SOIC-16 | Level-2-260C-1 YEAR | 1500 |
| 1401BRWZ | -40 ~125°C | 4 | 0 | 5 | Low | WB SOIC-16 | Level-2-260C-1 YEAR | 1500 |
| 1401BRWQ | -40 ~125°C | 4 | 0 | 5 | Low | WB SOIC-16 | Level-2-260C-1 YEAR | 1500 |
| 1403BRWH | -40 ~125°C | 3 | 1 | 5 | High | WB SOIC-16 | Level-2-260C-1 YEAR | 1500 |
| 1403BRWQ | -40 ~125°C | 3 | 1 | 5 | High | WB SOIC-16 | Level-2-260C-1 YEAR | 1500 |
| 1403BRWZ | -40 ~125°C | 3 | 1 | 5 | Low | WB SOIC-16 | Level-2-260C-1 YEAR | 1500 |
| 1403ARWQ | -40 ~125°C | 3 | 1 | 5 | Low | WB SOIC-16 | Level-2-260C-1 YEAR | 1500 |
| 1402ARWZ | -40 ~125°C | 2 | 2 | 5 | High | WB SOIC-16 | Level-2-260C-1 YEAR | 1500 |
| 1402ARWQ | -40 ~125°C | 2 | 2 | 5 | High | WB SOIC-16 | Level-2-260C-1 YEAR | 1500 |
| 1402BRWZ | -40 ~125°C | 2 | 2 | 5 | Low | WB SOIC-16 | Level-2-260C-1 YEAR | 1500 |
| 1402BRWQ | -40 ~125°C | 2 | 2 | 5 | Low | WB SOIC-16 | Level-2-260C-1 YEAR | 1500 |
| 1301ARWH | -40 ~125°C | 4 | 0 | 3 | High | 16-Lead SSOP | Level-3-260C-168 HR | 4000 |
| 1301ARWZ | -40 ~125°C | 4 | 0 | 3 | Low | 16-Lead SSOP | Level-3-260C-168 HR | 4000 |
| 1303ARWH | -40 ~125°C | 3 | 1 | 3 | High | 16-Lead SSOP | Level-3-260C-168 HR | 4000 |
| 1303ARWZ | -40 ~125°C | 3 | 1 | 3 | Low | 16-Lead SSOP | Level-3-260C-168 HR | 4000 |



| Model Name | Temperature Range | No. of Inputs, V _{DD1} Side | No. of Inputs, V _{DD2} Side | Withstand Voltage Rating (kV rms) | Fail-Safe Output State | Package | MSL Peak Temp | Quantity per reel |
|------------|-------------------|--------------------------------------|--------------------------------------|-----------------------------------|------------------------|--------------|---------------------|-------------------|
| 1302ARWH | -40 ~125°C | 2 | 2 | 3 | High | 16-Lead SSOP | Level-3-260C-168 HR | 4000 |
| 1302ARWZ | -40 ~125°C | 2 | 2 | 3 | Low | 16-Lead SSOP | Level-3-260C-168 HR | 4000 |