Multi-Mode PWM Power Switch with Integrated Protections

Features

- Built-in 650V Power MOSFET
- Low Start-Up Current (<2uA)
- Multi-Mode Operation
  CCM @ Heavy Load and Low Line
  QR-Like Operation @ Medium Load
  Green mode with Valley Skip at Light Load
  Burst Mode at No Load
- Accurate Over Current Protection
- Adjustment OVP on QRD Pin
- Output Short Protection
- Soft Driver
- 8ms Soft-start
- OVP (Over Voltage Protection) on Vcc Pin
- On Chip OTP Protection
- SOP-7 and DIP-8 Package with Few External Components Needed

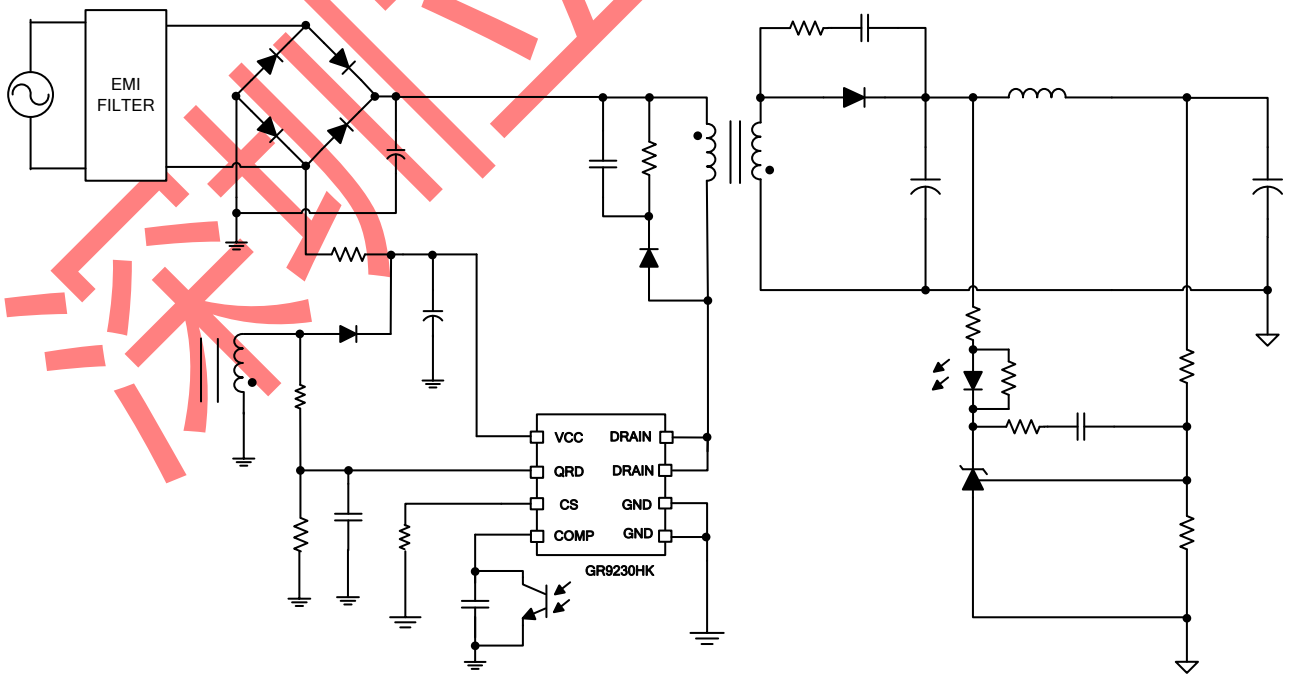
Description

The GR9230HK is integrates a high performance multi-mode (QR/CCM) PWM controller and a high voltage power MOSFET of 650V. It minimizes the components counts and is available in a tiny DIP-8 package. Those make it an ideal design for low cost application. It provides functions of low startup current, green- mode power-saving operation, VCC over-voltage protection, and QRD pin abnormal conditions sensing to prevent the circuit being damaged from the abnormal conditions.

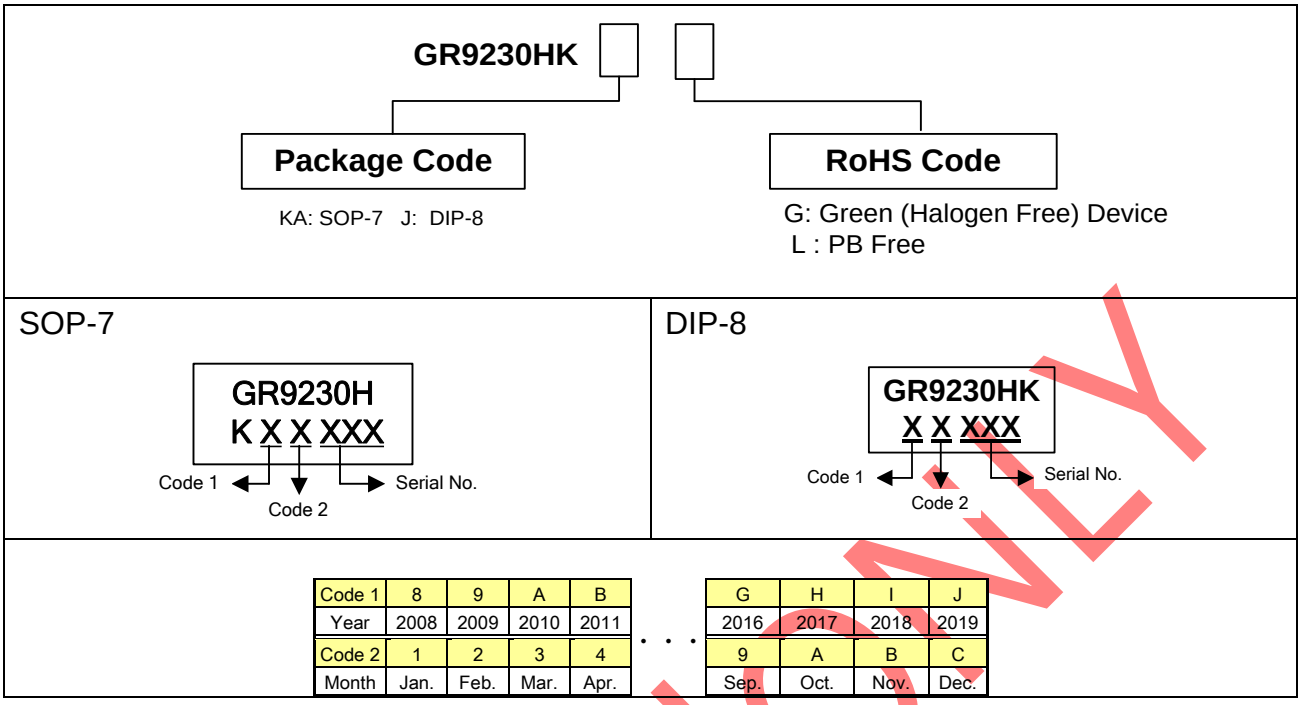
Applications

- Switching AC/DC power adapter
- SMPS Power Supply

Typical Application Information



Ordering and Marking Information



Code 1	8	9	A	B
Year	2008	2009	2010	2011
Code 2	1	2	3	4
Month	Jan.	Feb.	Mar.	Apr.

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G	H	I	J
2016	2017	2018	2019
9	A	B	C
Sep.	Oct.	Nov.	Dec.

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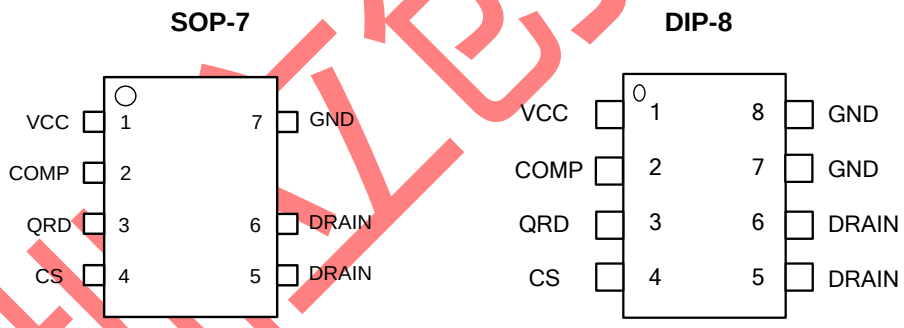
Pin Configuration(TOP VIEW)



Pin Description

Pin No.		Name	Function
SOP-7	DIP-8		
1	1	VCC	Power supply pin
2	2	COMP	Voltage feedback pin, by connecting a photo-coupler to control the duty cycle
3	3	QRD	This pin is for quasi-resonant detection and OVP.
4	4	CS	Current sense pin, connected to sense resistor for sensing the MOSFET current signal
5,6	5,6	DRAIN	Drain of internal HV MOSFET
7	7,8	GND	Ground reference pin

Absolute Maximum Ratings

Drain Voltage ---------- -0.3V ~ 650V

Supply voltage VCC ---------- 30V

COMP, CS, QRD---------- -0.3~6.0V

Junction temperature ---------- 150℃

Storage temperature range ---------- -65℃ ~ 150 ℃

Lead temperature (DIP-8, soldering, 10 sec) ---------- 230℃

Lead temperature (All Pb free packages, soldering, 10 sec) ---------- 260℃

ESD, human body model ---------- 2.5KV

ESD, machine model ---------- 250V

Thermal Resistance from Junction to ambient (SOP7, θJA) ---------- 150°C/W

Thermal Resistance from Junction to case (SOP7, θJC) ---------- 60°C/W

Caution: 1.The “Absolute Maximum Ratings” are those values beyond which the safety of the device cannot be guaranteed and may cause permanent damage to the IC. These are stress ratings only and functional operation of the device at these or any other condition beyond those indicated in the Electrical Characteristics section of the specification is not implied. The “Electrical Characteristics” table defines the conditions for actual device operation. Exposure to absolute maximum rated conditions for extended periods may affect device reliability 2. Thermal Resistance is a reference value. This value is recommended by applications and PCB design.

Recommended Operating Conditions

Item	Min.	Max.	Unit
Operating Junction temperature	-40	125	℃
Operating ambient temperature	-40	85	℃
Start Up Resistor (AC Half side)	540k	2.2M	Ω
Supply voltage VCC	9	26.5	V
VCC Capacitor	2.2	10	μF
COMP pin paralleling capacitor	1	33	nF
QRD Pin paralleling capacitor	4.7	33	pF

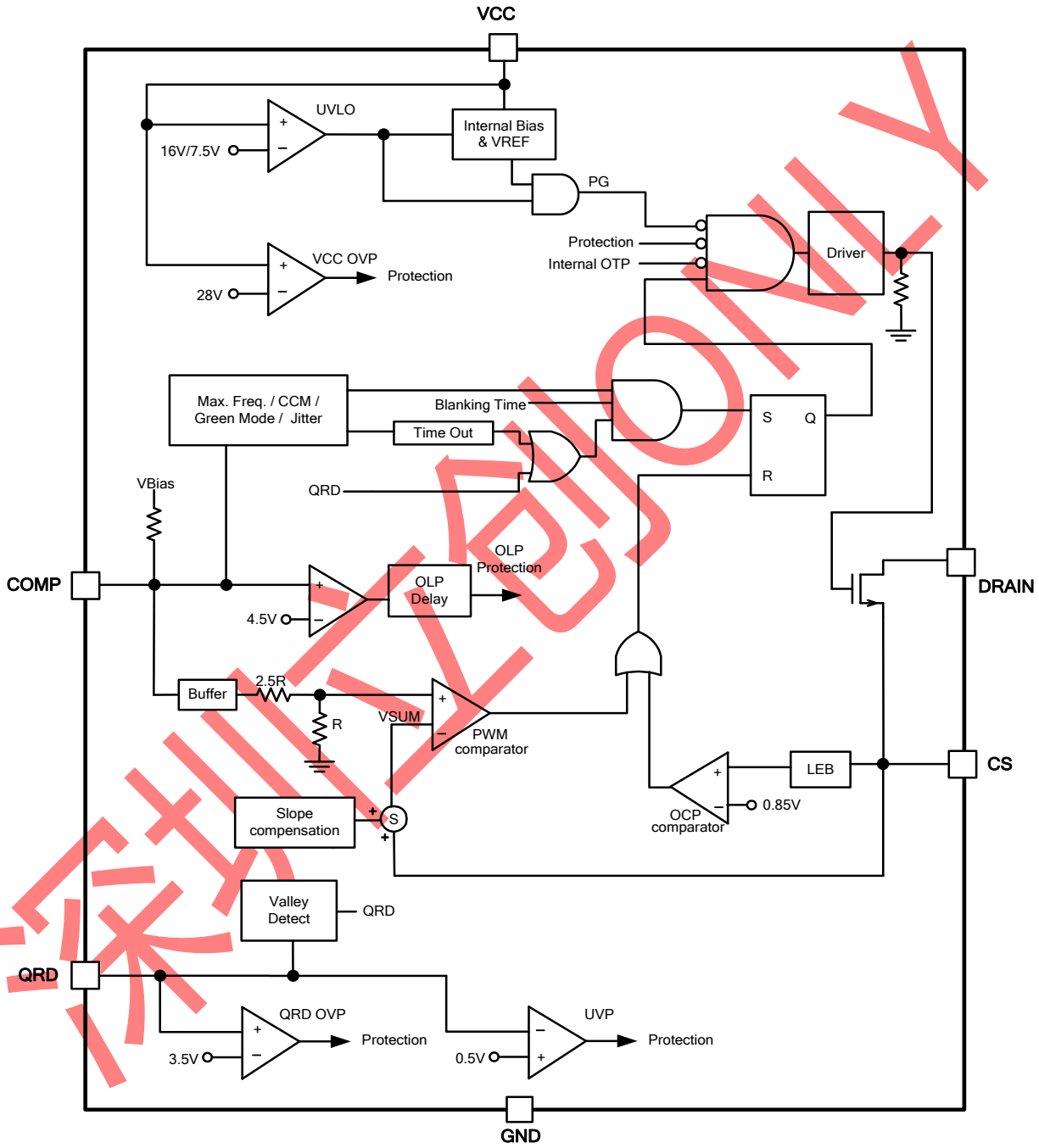
Note:

- Not to exceed the maximum junction temperature of the IC, this relates to the operating power of the IC and the thermal resistance of the IC-package as above.
- The small signal components should be placed to IC pin as possible.
- It’s essential to connect VCC pin with a SMD ceramic capacitor (0.1μF~0.47μF) to filter out the undesired switching noise for stable operation.
- Suggest using electrolytic capacitor or 1206 SMD ceramic capacitor as the VCC capacitor to avoid the acoustic noise from MLCC piezoelectric effect.
- Connecting a capacitor to COMP pin is also essential to filter out the undesired switching noise for stable operation.
- Connecting a capacitor (4.7~33pF) to QRD pin is also essential to filter out the undesired switching noise for stable operation.

Protection Mode

CCM Switching Frequency	OLP/UVP	VCC OVP	QRD OVP
100kHz	Auto recovery	Auto recovery	Auto recovery

Block Diagram



Electrical Characteristics (TA = +25℃ unless otherwise stated, VCC = 15.0V)

Parameter	Min.	Typ.	Max.	Unit
SUPPLY VOLTAGE (VCC Pin)				
Startup current VCC=UVLO ON-0.1V	0.75	1.5	2	uA
Operating current , Vcomp = 0V		0.65		mA
Operating current , Vcomp = 2.5V		2.1		mA
Operating current, protection tripped (VCC OVP, FB UVP)		0.65		mA
UVLO-OFF	7.0	7.5	8.0	V
UVLO-ON	15.2	16.0	16.8	V
VCC Mode Entry Point		8.5		V
Hysteresis		0.25		V
OVP level on VCC pin		28		V
OVP level on VCC pin Debounce Time*		128		μs
VOLTAGE FEEDBACK (COMP Pin)				
Short circuit current, Vcomp = 0V		230		uA
Open loop voltage, COMP pin open	4.8	5.2	5.6	V
Maximum Frequency Threshold, V_{SMAX}*		1.9		V
Green Mode Threshold*		1.49		V
CURRENT SENSING (CS Pin)				
Maximum input voltage at Low Line, Vcsmax(ON Time>4us*)	0.80	0.85	0.90	V
Maximum input voltage at High Line, VcsmaxL (ON Time<3us*)		0.7		V
Internal Slope Compensation*		0.3		V
Leading-edge blanking time		300		ns
Input impedance	1			MΩ
Delay to Output*		100		ns
QRD (QRD Pin)				
Upper Clamp Level, IZCD=0.5mA		4.6		V
Lower Clamp Level, IZCD=-0.3mA		-0.3		V
QRD Blanking Time		2.0		μs
QRD OVP	3.38	3.5	3.62	V
OVP De-bounce Time*		64		μs
UVP Level		0.5		V
UVP De-bounce Time after start-up*		8		ms

Electrical Characteristics (T_A = +25℃ unless otherwise stated, VCC = 15.0V)

Parameter	Min.	Typ.	Max.	Unit
OSCILLATOR				
CCM Frequency	92	100	108	kHz
Maximum Frequency Clamp, Vcomp>V_{SMAX}		106		kHz
Green Mode Frequency		23		kHz
Jitter Frequency (CCM, Vcomp>Vsmax)		±8		%
Soft Start Time (CS Pin)				
Soft Start Time*		8		ms
PWM SECTION				
Maximum On Time		6.8		μs
Open Loop Protection (COMP Pin)				
OLP trip level, Vcomp	4.2	4.35	4.5	V
OLP delay time after start-up	55	69	84	ms
Internal OTP (Guaranteed by design)				
OTP*		145		℃
Hysteresis*		30		℃
MOSFET SECTION				
BVdss Vgs=0	650			V
Rds (on)		2.6		Ω

*Guaranteed by Design.

Application Information

Overview

The GR9230HK is integrates a high performance multi-mode (QR/CCM) PWM controller and a high voltage power MOSFET of 650V This results in a low-cost solution for low power AC/DC adapters. It integrated more functions to reduce the external components counts and the size. Its major features are described as below.

Start-up Current

The typical start-up current is 1.5uA. Very low start-up current allows the PWM power switch to increase the value of start-up resistor and then reduce the power dissipation on it.

Under-voltage Lockout (UVLO)

A hysteresis UVLO comparator is implemented in GR9230HK, then the turn-on and turn-off thresholds level are fixed at 16V and 7.5V respectively. This hysteresis shown in Fig.1 ensures that the start-up capacitor will be adequate to supply the chip during start-up.

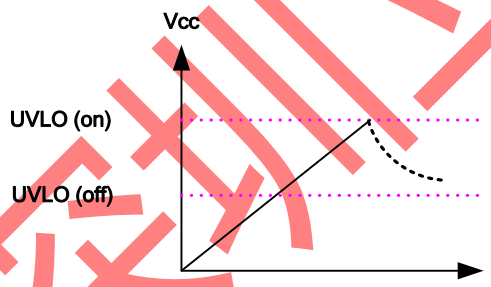


Fig.1

Multi-Mode Operation for High Efficiency

GR9230HK is a multi-mode QR/CCM controller. The controller changes the mode of operation according to switching frequency and comp pin voltage, as shown in the Fig.2. At the normal operating condition, the IC operates in QR mode to reduce the switching loss. In the QR mode, the frequency varies depending on the line voltage and the load conditions. As the output load current is increased, the on-time T_{ON} is increased, and thus the switching frequency decreases. If the switching frequency lowers than 100kHz frequency, the controller adaptively transitions to a CCM mode. Thus, small size transformer can be used with high power conversion efficiency.

As the output load current is decreased, the on-time T_{ON} is decreased, and thus the switching frequency increases. If the switching frequency increases till over the clamp of 106kHz, IC will skip the first valley to turn on in 2nd or 3rd valley.

At light load conditional, the VCOMP is lower than V_{SG1} and the system operates in green mode for high power conversion efficiency. The max switching frequency clamp will start to linearly decrease from 106kHz to 23kHz. The valley switching characteristic is still preserved in green mode. That is, when load decreases, the system automatically skip more and more valleys and the switching frequency is thus reduced.

At zero load or very light load conditions (Vcomp< Burst mode voltage), the gate output pin of the GR9230HK will be disabled immediately under such condition, enhancing power saving.

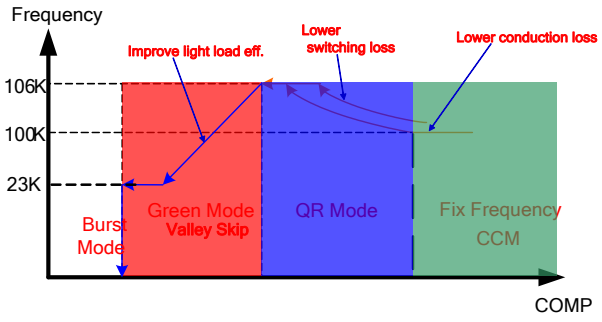


Fig.2

Quasi-Resonant Detection

The QR detection block will detect auxiliary winding voltage to turn on the MOSFET. It can decrease power loss of turn-on for high efficiency.

Leading-edge Blanking (LEB)

Each time the power MOSFET is switched on, a turn-on spike will inevitably occur at the sense resistor. To avoid fault trigger, a leading-edge blanking time is built in. During this blanking period, the current-limit comparator is disabled and cannot switch off the gate driver.

Internal Slope Compensation

A built-in slope compensation circuit is constructed in GR9230HK. When the switch is on, a ramp voltage is added to the sensed voltage across the CS pin, which helps to stabilize the system and prevent sub-harmonic oscillations.

Over-voltage Protection (OVP) on Auto Recovery mode

To prevent power MOSFET from being damaged, the GR9230HK is implemented an OVP function on VCC. When the VCC voltage is higher than the OVP threshold voltage, the output gate driver circuit will be shut down immediately to stop the switching of power MOSFET. The VCC OVP function is an auto-recovery type protection. If OVP happens, the pulses will be stopped and recover at the next UVLO on. The GR9230HK is working in a hiccup mode as shown in Fig. 3.

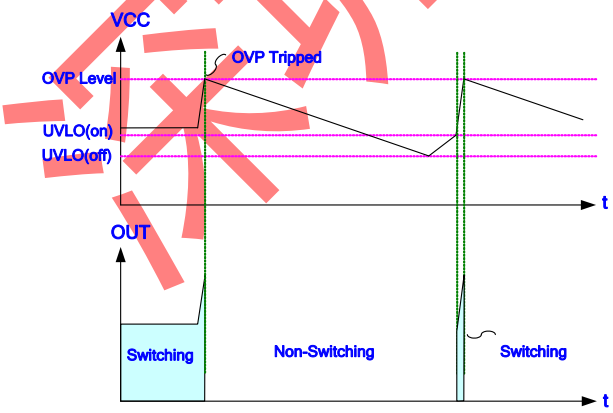


Fig.3

Output OVP on QRD - Auto Recovery mode

An output overvoltage protection is implemented in the GR9230HK, as shown in Fig. 4 and 5. It senses the auxiliary voltage via the divided resistors. The overvoltage protection works by sampling the plateau voltage after a delay time. The sampling voltage level is compared with internal threshold voltage 3.5V. If the sampling voltage exceeds the QRD OVP trip level, the QRD OVP circuit switches the power MOSFET off. The QRD OVP function is an auto-recovery type protection. The de-bounce time of QRD OVP is 64μs to prevent incorrect OVP detection which might occur during ESD or lightning events.

Output Under-voltage Protection (UVP) on QRD– Auto Recovery mode

To protect the circuit from damage due to output short condition, an auto-recovery type of UVP protection is implemented for it. If the QRD voltage declines below 0.5V for over the 8ms, the protection will be activated to turn off the gate until the next UVLO-ON.

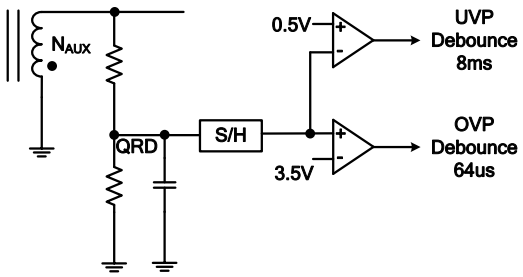


Fig.4

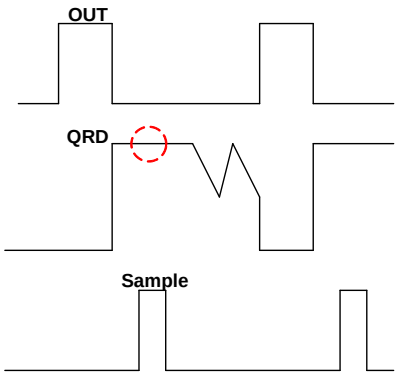


Fig.5

OLP (Open Loop Protection) – Auto Recovery mode

The GR9230HK has open loop protection function. An internal circuit detects the Vcomp level, when the Vcomp is larger than an OLP threshold level and continues over OLP delay time, the protection will be activated and then turn off the gate output to stop the switching of power circuit. Then VCC decreases below UVLO off level, the controller resets again.

Gate Clamp/Soft Driving

Driver output is clamped by an internal 13.5V clamping circuit to prevent from undesired over-voltage gate signals. And under the conditions listed below, the gate output will turn off immediately to protect the power circuit. The GR9230HK also has soft driving function to minimize EMI.

VCC Mode Operation

In order to avoid the output voltage shut down by load changing from full to no load, the GR9230HK is built-in the VCC mode function. When the load from full changes to no load, the output voltage will overshoot and pull low the COMP pin by feedback loop (Into burst mode). Thus the duty will disappear and no power delivers to the secondary. If there is without any mechanism to prevent this situation, the VCC pin voltage will down to UVLO off and the IC will re-start again. In the GR9230HK, before the VCC is down to UVLO off, it will force the OUT pin outputs the specified duty to pull the VCC higher than UVLO off.

The VCC mode function is used to prevent the output re-start again when load changes. So never let the system operate on the VCC mode at no load. The system should operate on burst mode, otherwise the input power maybe become larger.

Fault Protection

There are several critical protections integrated in the

. CS pin floating

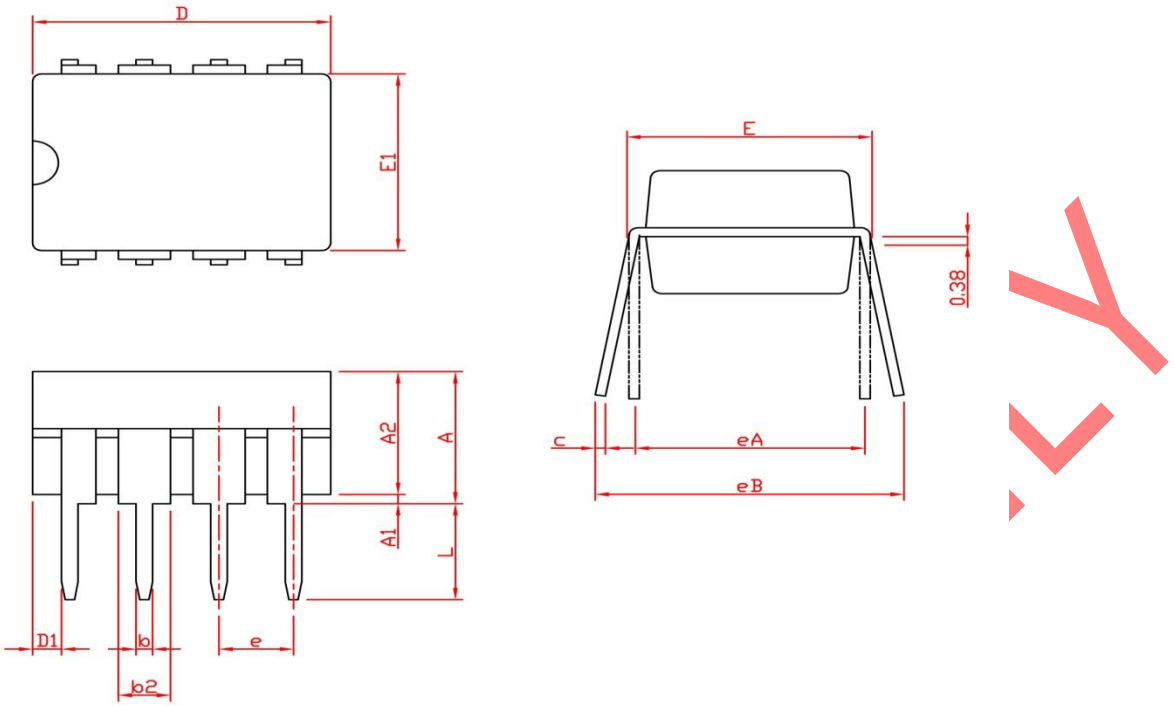
. Comp pin shorting

. Comp pin floating

. QRD pin shorting

Package Information

DIP-8



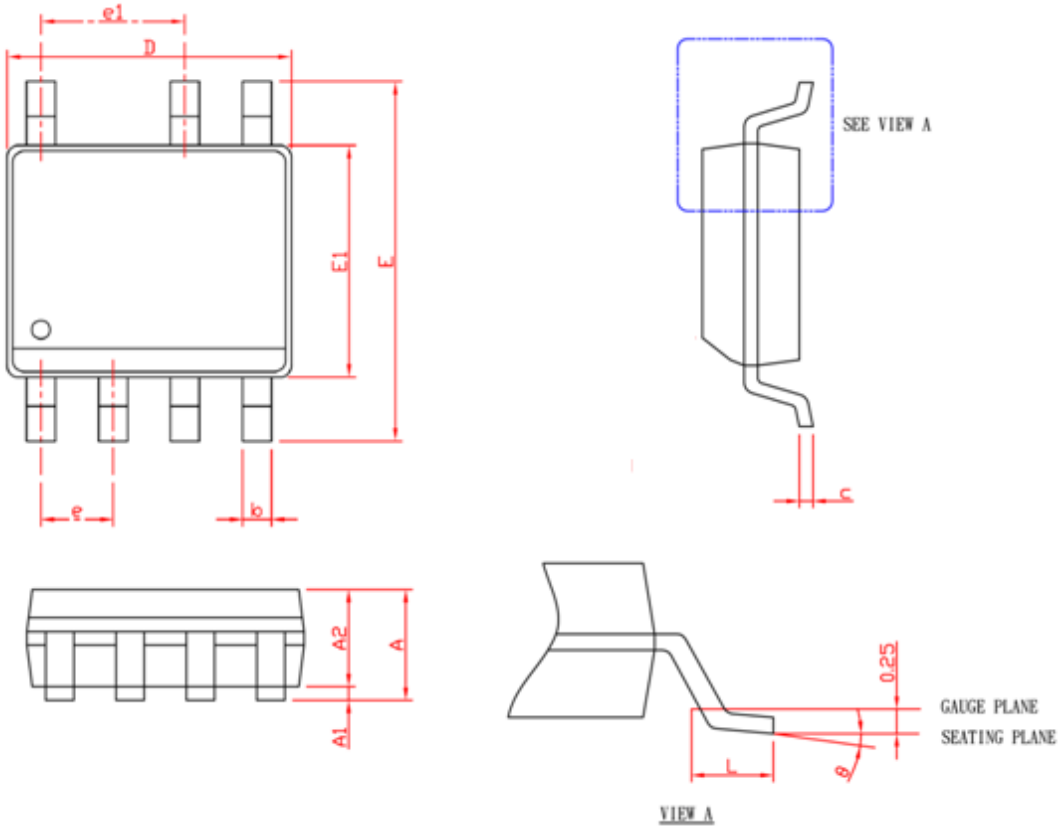
SYMBOL	DIP-8			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A		5.33		0.210
A1	0.38		0.015	
A2	2.92	4.95	0.115	0.195
b	0.36	0.56	0.014	0.022
b2	1.14	1.78	0.045	0.070
c	0.20	0.35	0.008	0.014
D	9.01	10.16	0.355	0.400
D1	0.13		0.005	
E	7.62	8.26	0.300	0.325
E1	6.10	7.11	0.240	0.280
e	2.54 BSC		0.100 BSC	
eA	7.62 BSC		0.300 BSC	
eB		10.92		0.430
L	2.92	3.81	0.115	0.150

Note: 1. Followed from JEDEC MS-001 BA.

2. Dimension D, D1 and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 10 mil.

Package Information

SOP-7



SYMBOL	SOP-7	
	MILLIMETERS	
	MIN.	MAX.
A		1.75
A1	0.10	0.25
A2	1.25	
b	0.31	0.51
c	0.10	0.25
D	4.70	5.10
E	5.80	6.20
E1	3.70	4.10
e	1.27 BSC	
e1	2.54 BSC	
L	0.40	1.27
θ	0^o	8^o

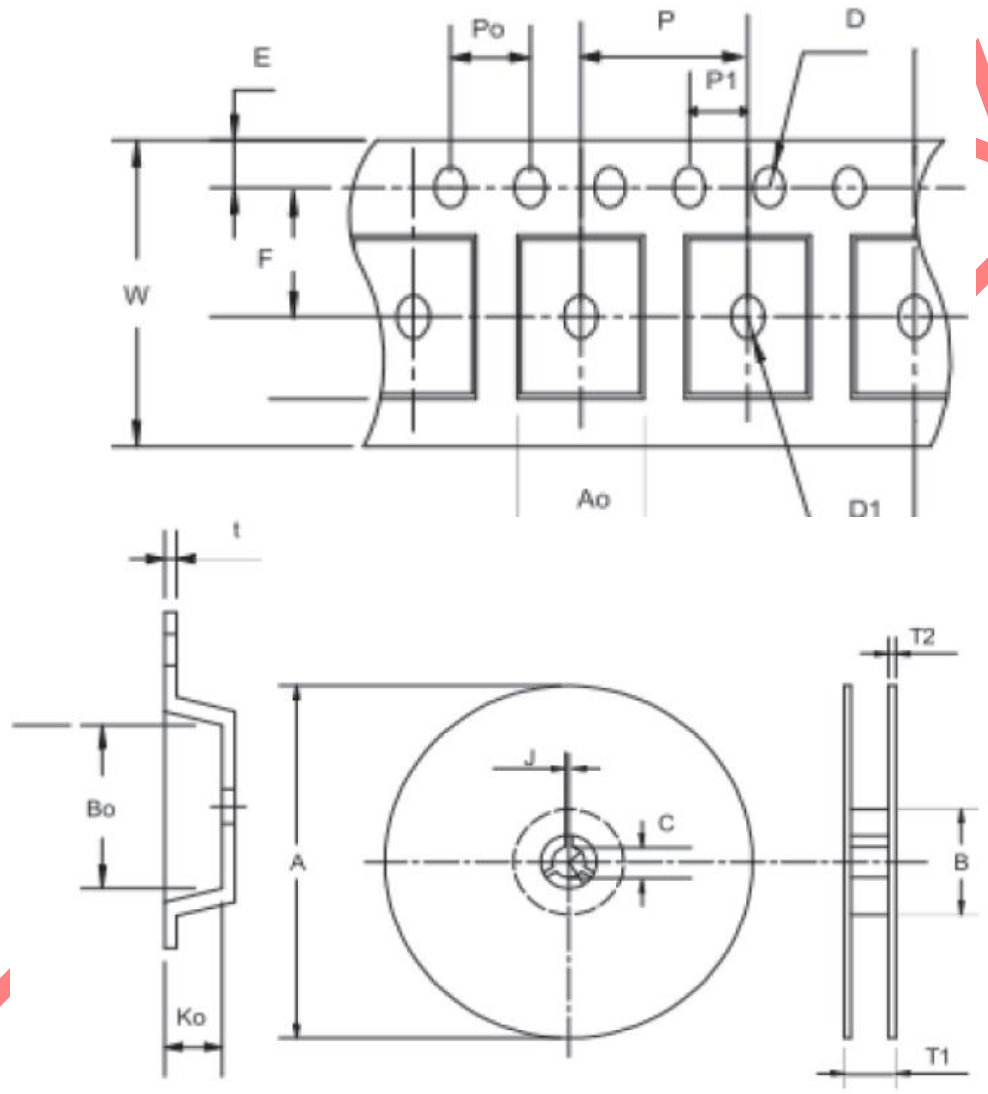
Note: 1. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusion or gate burrs shall not exceed 6 mil per side.

2. Dimension “E” does not include inter-lead flash or protrusions. Inter-lead flash and protrusions shall

not exceed 10 mil per side.

Carrier Tape & Reel Dimensions

SOP- 7



PKG TYPE	W	E	F	P0	A0	P	P1	B0	K0	A	B	T1
SOP-7/ 8/8P	12±0.3	1.75±0.1	5.5±0.05	4±0.1	6.4±0.2	8±0.1	2±0.2	5.2±0.2	2.1±0.2	330±2	50min	12.4+2/-0

Devices Per Unit

Application	Carrier Width	Devices Per Reel
SOP- 7	12	2500

Tape and Specification Reel

SOP-7