

ITS4200S-ME-N

Smart High-Side NMOS-Power Switch

Data Sheet

Rev 1.0, 2012-09-01

Standard Power



1 Overview

Features

- CMOS compatible input
- Switching all types of resistive, inductive and capacitive loads
- Fast demagnetization of inductive loads
- Very low standby current
- Optimized Electromagnetic Compatibility
- Overload protection
- Current limitation
- Short circuit protection
- Thermal shutdown with restart
- Overvoltage protection (including load dump)
- Reverse battery protection with external resistor
- Loss of GND and loss of Vbb protection
- Electrostatic Discharge Protection (ESD)
- Green Product (RoHS compliant)

ITS4200S-ME-N is not qualified and manufactured according to the requirements of Infineon Technologies with regards to automotive and/or transportation applications.

Description

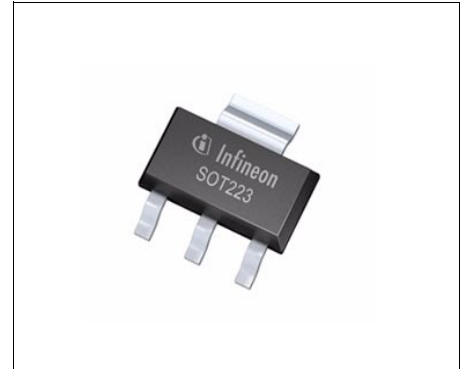
The ITS4200S-ME-N is a protected single channel Smart High-Side NMOS-Power Switch in a SOT-223-4 package with charge pump and CMOS compatible input. The device is monolithically integrated in Smart technology.

Product Summary

Overvoltage protection $V_{SAZ\ min} = 41V$
 Operating voltage range: $5V \leq V_S \leq 34V$
 On-state resistance $R_{DSON\ typ} = 160m\Omega$
 Nominal load current $I_{LNOM} = 0.7A$
 Operating Temperature range: $T_j = -40^\circ C$ to $125^\circ C$
 Standby Current: $I_{SSTB} = 25\mu A$

Application

- All types of resistive, inductive and capacitive loads
- Power switch for 12V and 24V DC applications with CMOS compatible control interface
- Driver for electromagnetic relays
- Power management for high-side-switching with low current consumption in OFF-mode



SOT-223-4

Type	Package	Marking
ITS4200S-ME-N	SOT-223-4	I200SN

2 Block Diagram and Terms

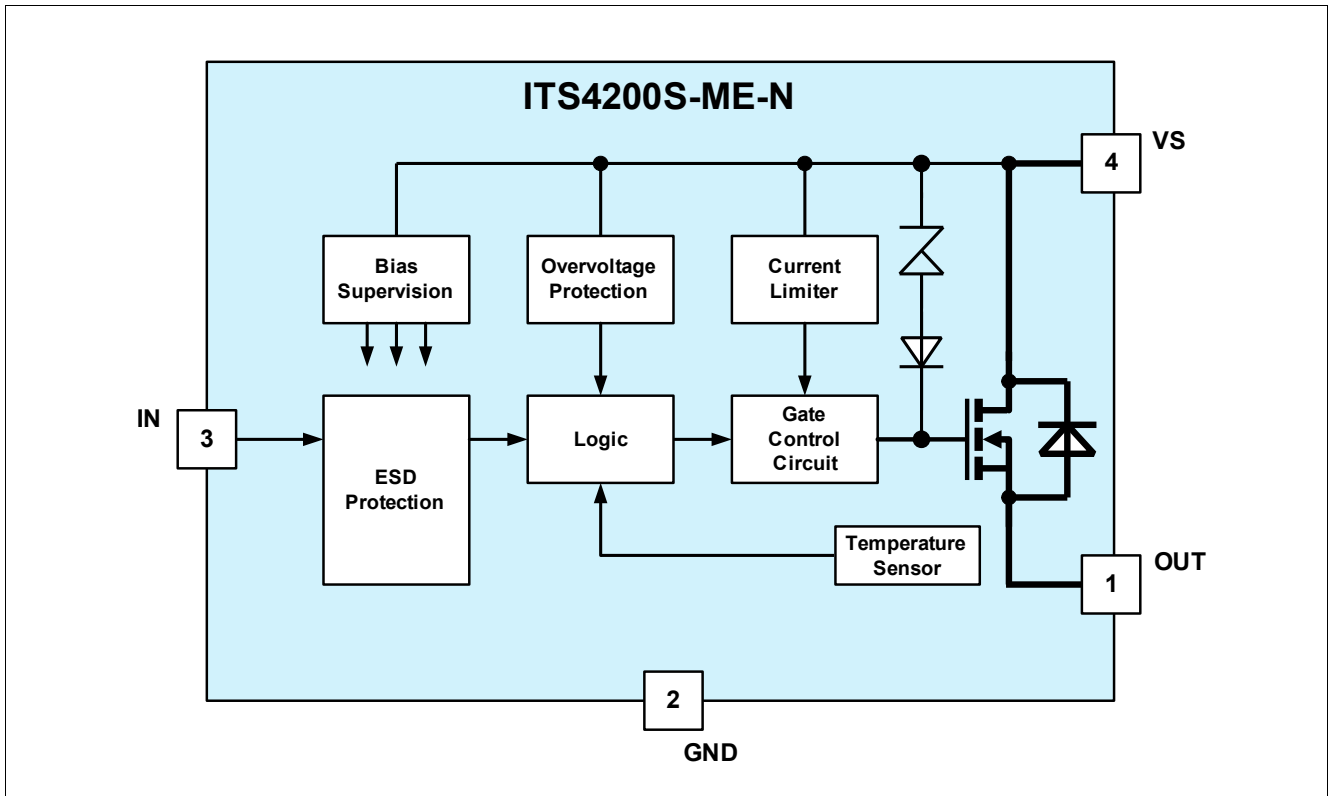


Figure 1 Block diagram

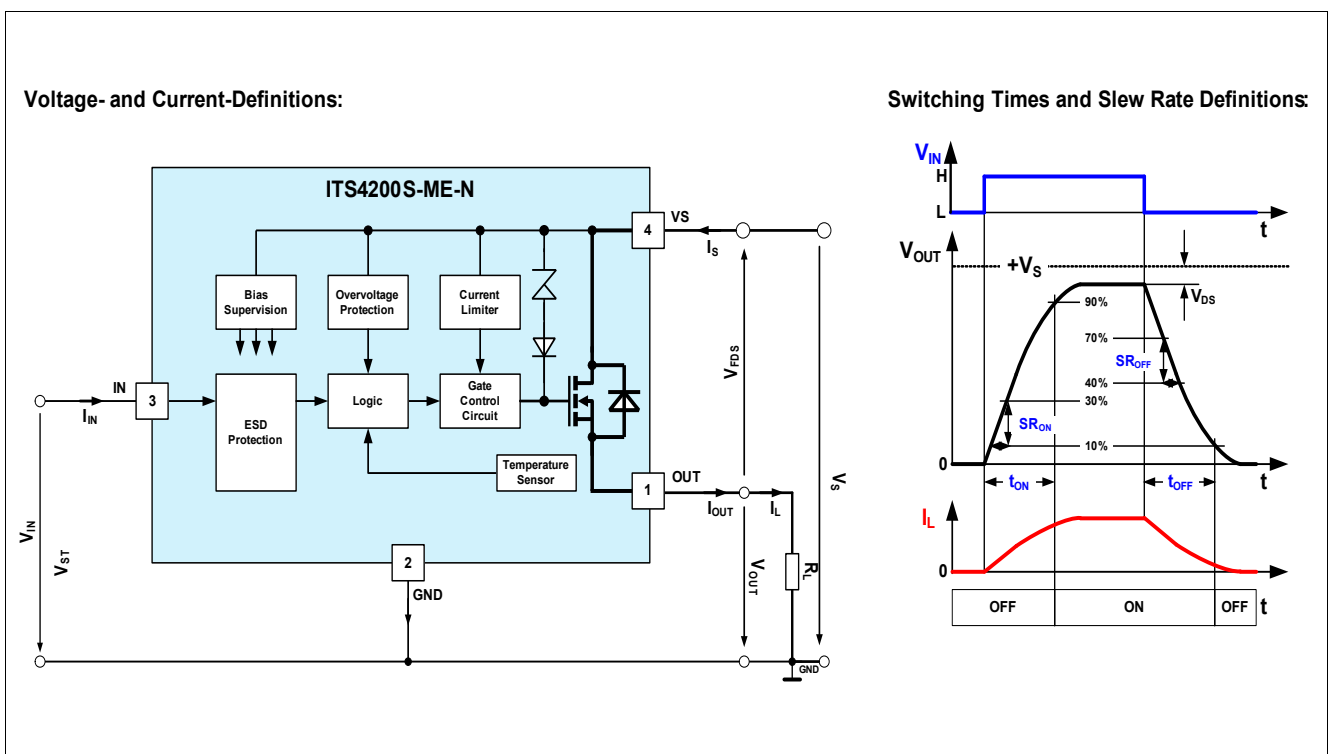


Figure 2 Terms - parameter definition

3 Pin Configuration

3.1 Pin Assignment

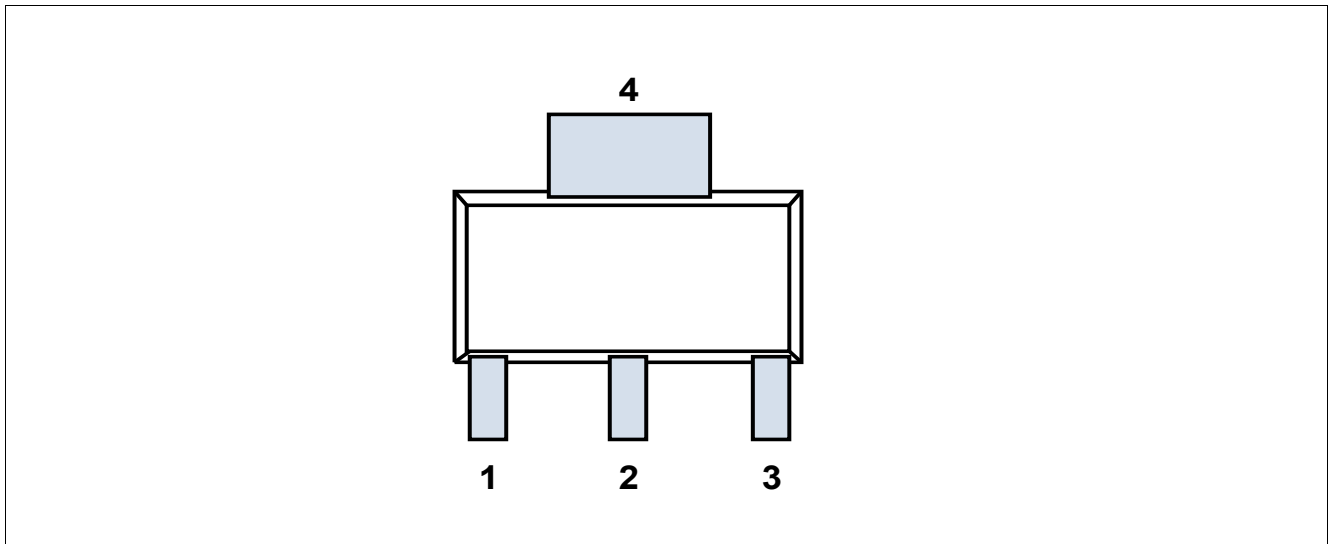


Figure 3 Pin configuration top view, SOT-223-4

3.2 Pin Definitions and Functions

Pin	Symbol	Function
1	OUT	Output to the load
2	GND	Logic ground
3	IN	Input, controls the power switch; the powerswitch is ON when high
4	VS	Supply voltage (design the wiring for the maximum short circuit current and also for low thermal resistance)

4 General Product Characteristics

4.1 Absolute Maximum Ratings

Table 1 Absolute maximum ratings²⁾ at $T_j = 25^\circ\text{C}$ unless otherwise specified. Currents flowing into the device unless otherwise specified in chapter "Block Diagram and Terms"

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Supply voltage VS							
Voltage	V_S	–	–	40	V		4.1.1
Output stage OUT							
Output Current; (Short circuit current see electrical characteristics)	I_{OUT}	self limited			A		4.1.2
Input IN							
Voltage	V_{IN}	-5	–	V_S	V		4.1.3
Current	I_{IN}	-5	–	5	mA		4.1.4
Temperatures							
Junction Temperature	T_j	-40	–	125	$^\circ\text{C}$		4.1.5
Storage Temperature	T_{stg}	-55	–	125	$^\circ\text{C}$		4.1.6
Power dissipation							
$T_a = 25^\circ\text{C}^{1)}$	P_{tot}	–	–	1.4	W		4.1.7
Inductive load switch-off energy dissipation							
$T_j = 125^\circ\text{C}; V_S = 13.5\text{V}; I_L = 0.5\text{A}^{2)}$	E_{AS}	–	–	500	mJ	single pulse	4.1.8
ESD Susceptibility							
ESD susceptibility (input pin)	V_{ESD}	-1	–	1	kV	HBM ³⁾	4.1.9
ESD susceptibility (all other pins)	V_{ESD}	-2	–	2	kV	HBM ³⁾	4.1.10

1) Device on 50mm*50mm*1.5mm epoxy PCB FR4 with 6 cm² (one layer, 70mm thick) copper area for V_{bb} connection. PCB is vertical without blown air

2) Not subject to production test, specified by design

3) ESD susceptibility HBM according to EIA/JESD 22-A 114.

Note: Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Integrated protection functions are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as "outside" the normal operating range. Protection functions are neither designed for continuous nor repetitive operation.

4.2 Functional Range

Table 2 Functional Range

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Nominal Operating Voltage	V_S	5	–	34	V	V_S increasing	4.2.1
Continuous Input Voltage	V_{IN}	-3	–	V_S	V		4.2.2

Note: Within the functional range the IC operates as described in the circuit description. The electrical characteristics are specified within the conditions given in the related electrical characteristics table.

4.3 Thermal Resistance

This thermal data was generated in accordance to JEDEC JESD51 standards.

More information on www.jedec.org

Table 3 Thermal Resistance¹⁾

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Thermal Resistance - Junction to pin5	$R_{thj-pin5}$	–	35.0	–	K/W		4.3.1
Thermal Resistance - Junction to Ambient - 1s0p, minimal footprint	R_{thJA_1s0p}	–	120.0	–	K/W	²⁾	4.3.2
Thermal Resistance - Junction to Ambient - 1s0p, 300mm ²	$R_{thJA_1s0p_300mm^2}$	–	69.3	–	K/W	³⁾	4.3.3
Thermal Resistance - Junction to Ambient - 1s0p, 600mm ²	$R_{thJA_1s0p_600mm^2}$	–	61.6	–	K/W	⁴⁾	4.3.4
Thermal Resistance - Junction to Ambient - 2s2p	R_{thJA_2s2p}	–	55.5	–	K/W	⁵⁾	4.3.5
Thermal Resistance - Junction to Ambient with thermal vias - 2s2p	R_{thJA_2s2p}	–	48.3	–	K/W	⁶⁾	4.3.6

1) Not subject to production test, specified by design

2) Specified R_{thJA} value is according to Jedec JESD51-3 at natural convection on FR4 1s0p board, footprint; the Product (Chip+Package) was simulated on a 76.2 x 114.3 x 1.5 mm board with 1x 70µm Cu.

3) Specified R_{thJA} value is according to Jedec JESD51-3 at natural convection on FR4 1s0p board, Cu, 300mm²; the Product (Chip+Package) was simulated on a 76.2 x 114.3 x 1.5 mm board with 1x 70µm Cu.

4) Specified R_{thJA} value is according to Jedec JESD51-3 at natural convection on FR4 1s0p board, 600mm²; the Product (Chip+Package) was simulated on a 76.2 x 114.3 x 1.5 mm board with 1x 70µm Cu.

5) Specified R_{thJA} value is according to Jedec JESD51-2,-5,-7 at natural convection on FR4 2s2p board; the Product (Chip+Package) was simulated on a 76.2 x 114.3 x 1.5 mm board with 2 inner copper layers (2 x 70µm Cu, 2 x 35µm Cu).

General Product Characteristics

- 6) Specified R_{thJA} value is according to Jedec JESD51-2,-5,-7 at natural convection on FR4 2s2p board with two thermal vias; the Product (Chip+Package) was simulated on a 76.2 x 114.3 x 1.5 mm board with 2 inner copper layers (2 x 70 μ m Cu, 2 x 35 μ m Cu). The diameter of the two vias are equal 0.3mm and have a plating of 25 μ m with a copper heatsink area of 3mm x 2mm). JEDEC51-7: The two plated-through hole vias should have a solder land of no less than 1.25 mm diameter with a drill hole of no less than 0.85 mm diameter.

5 Electrical Characteristics

Table 4 $V_S = 13.5V$; $T_j = 25^\circ C$; all voltages with respect to ground, currents flowing into the device unless otherwise specified in chapter "Block Diagram and Terms". Typical values at $V_S = 13.5V$, $T_j = 25^\circ C$

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Powerstage							
NMOS ON Resistance	R_{DSON}	–	160	200	m Ω	$I_{OUT} = 0.5A$; $T_j = 25^\circ C$; $V_{IN} = 5V$	5.0.1
NMOS ON Resistance	R_{DSON}	–	–	400	m Ω	$I_{OUT} = 0.5A$; $T_j = 125^\circ C$; $V_{IN} = 5V$	5.0.2
Nominal Load Current; device on PCB ¹⁾	I_{LNOM}	0.7	–	–	A	$T_{pin5} = 85^\circ C$	5.0.3
Timings of Power Stages²⁾							
Turn ON Time(to 90% of V_{out}); L to H transition of V_{IN}	t_{ON}	–	60	100	μs	$V_S = 13.5V$; $R_L = 24\Omega$	5.0.4
Turn OFF Time (to 10% of V_{out}); H to L transition of V_{IN}	t_{OFF}	–	60	150	μs	$V_S = 13.5V$; $R_L = 24\Omega$	5.0.5
ON-Slew Rate (10 to 30% of V_{out}); L to H transition of V_{IN}	SR_{ON}	–	2	4	V / μs	$V_S = 13.5V$; $R_L = 24\Omega$	5.0.6
OFF-Slew Rate; dV_{OUT} / dt_{ON} (70 to 40% of V_{out}); H to L transition of V_{IN}	SR_{OFF}	–	2	4	V / μs	$V_S = 13.5V$; $R_L = 24\Omega$	5.0.7
Under voltage lockout (charge pump start-stop-restart)							
Supply undervoltage; charge pump stop voltage	V_{SUV}	3.5	–	5.0	V	V_S decreasing $T_j = -40^\circ C$ to $125^\circ C$	5.0.8
Supply startup voltage	V_{SSU}	–	–	6.5	V	V_S increasing $T_j = -40^\circ C$ to $25^\circ C$	5.0.9
Supply startup voltage	V_{SSU}	–	–	7.0	V	V_S increasing $T_j = 125^\circ C$	5.0.10
Supply startup voltage; Charge pump restart voltage	V_{SSCHP}	–	5.6	7.0	V	V_S increasing	5.0.11
Undervoltage hysteresis; $V_{UVHYS} = V_{SSU} - V_{SUV}$	V_{UVHYS}	–	0.3	–	V		5.0.12
Over voltage lockout							
Overvoltage shutdown threshold	V_{SOV}	34	–	42	V	V_S decreasing $T_j = -40^\circ C$ to $125^\circ C$	5.0.13
Overvoltage restart threshold	V_{SOVRS}	33	–	–	V	V_S decreasing $T_j = -40^\circ C$ to $125^\circ C$	5.0.14
Overvoltage hysteresis; $V_{OVHYS} = V_{SOCSD} - V_{SOVRS}$	V_{OVHYS}	–	0.7	–	V		5.0.15
Current consumption							

Electrical Characteristics

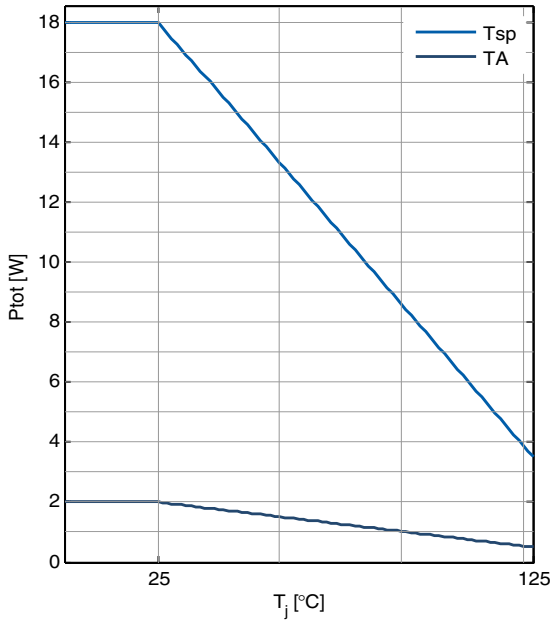
Table 4 $V_S = 13.5V$; $T_j = 25^\circ C$; all voltages with respect to ground, currents flowing into the device unless otherwise specified in chapter "Block Diagram and Terms". Typical values at $V_S = 13.5V$, $T_j = 25^\circ C$

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Operating current	I_{GND}	–	1.0	1.6	mA	$V_{IN} = 5V$	5.0.16
Standby current	I_{SSTB}	–	10	25	μA	$V_{IN} = 0V$; $V_{OUT} = 0V$; $T_j = -40^\circ C$ to $125^\circ C$	5.0.17
Output leakage current	I_{OUTLK}	–	2	5	μA	$V_{IN} = 0V$; $V_{OUT} = 0V$; $T_j = -40^\circ C$ to $25^\circ C$	5.0.18
Output leakage current	I_{OUTLK}	–	–	7	μA	$V_{IN} = 0V$; $V_{OUT} = 0V$; $T_j = 125^\circ C$	5.0.19
Protection functions ³⁾							
Initial peak short circuit current limit	I_{LSCP}	0.7	1.5	2.0	A	$T_j = 25^\circ C$; $V_S = 20V$; $V_{IN} = 5.0V$	5.0.20
Initial peak short circuit current limit	I_{LSCP}	0.7	–	2.4	A	$T_j = -40^\circ C$ to $125^\circ C$; $V_S = 20V$; $V_{IN} = 5.0V$	5.0.21
Output clamp at $V_{OUT} = V_S - V_{DSCL}$ (inductive load switch off)	V_{DSCL}	41	47	–	V	$I_S = 4mA$	5.0.22
Oversvoltage protection	V_{SAZ}	41	–	–	V	$I_S = 4mA$; $T_j = -40^\circ C$ to $125^\circ C$	5.0.23
Thermal overload trip temperature	T_{Jtrip}	150	–	–	$^\circ C$	–	5.0.24
Thermal hysteresis	T_{HYS}	–	10	–	K	–	5.0.25
Reverse Battery ⁴⁾							
Continuous reverse battery voltage	V_{SREV}	- 30	–	–	V	–	5.0.26
Input interface; pin IN							
Input turn-ON threshold voltage	V_{INON}	3.5	–	–	V	$T_j = -40^\circ C$ to $125^\circ C$	5.0.27
Input turn-OFF threshold voltage	V_{INOFF}	–	–	1.5	V	$T_j = -40^\circ C$ to $125^\circ C$	5.0.28
Input threshold hysteresis	V_{INHYS}	–	0.5	–	V	–	5.0.29
Off state input current	I_{INOFF}	10	–	60	μA	$V_{IN} = 1.2V$; $T_j = -40^\circ C$ to $125^\circ C$	5.0.30
On state input current	I_{INON}	10	–	100	μA	$V_{IN} = 3V$ to V_S ; $T_j = -40^\circ C$ to $125^\circ C$	5.0.31
Input resistance	R_{IN}	1.5	2.8	3.5	k Ω	–	5.0.32

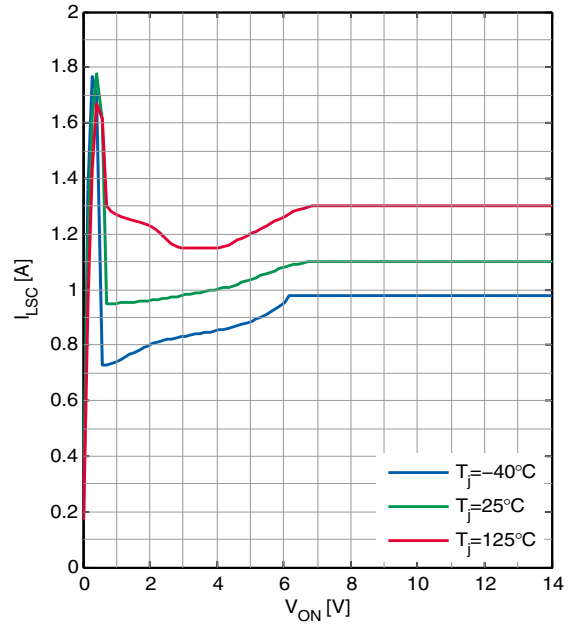
- 1) Device on 50mm x 50mm x 1,5mm epoxy FR4 PCB with 6cm² (one layer copper 70um thick) copper area for supply voltage connection. PCB in vertical position without blown air.
- 2) Timing values only with high slewrate input signal; otherwise slower.
- 3) Integrated protection functions are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as "outside" normal operating range. Protection functions are not designed for continuous repetitive operation.
- 4) Requires a 150W resistor in GND connection. The reverse load current trough the intrinsic drain-source diode of the power-MOS has to be limited by the connected load. Power dissipation is higher compared to normal operation due to the vottage drop across the drain-source diode. The temperature protection is not functional during reverse current operation! Input current has to be limited (see max ratings).

6 Typical Performance Graphs

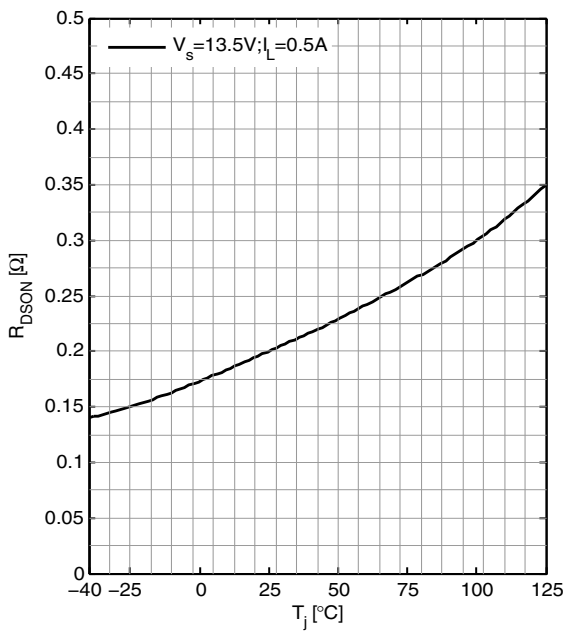
Maximal allowable Power Dissipation P_{tot} versus Ambient and Soldering Point Temperature T_a ; T_{SP}



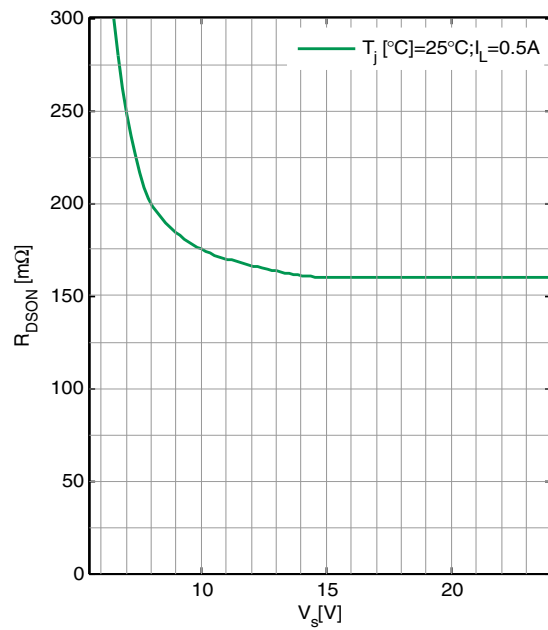
Initial Peak Short Circuit Current Limit I_{LSCP} versus Drain-Source Voltage V_{DS}



On-Resistance R_{DSON} versus Junction Temperature T_j

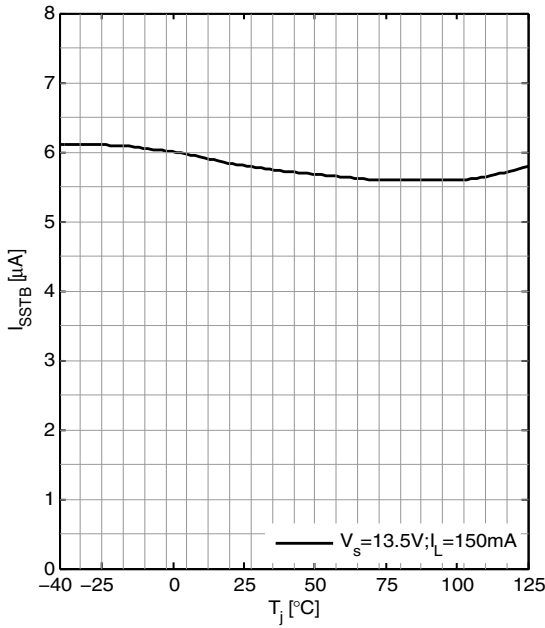


On-Resistance R_{DSON} versus Supply Voltage V_s

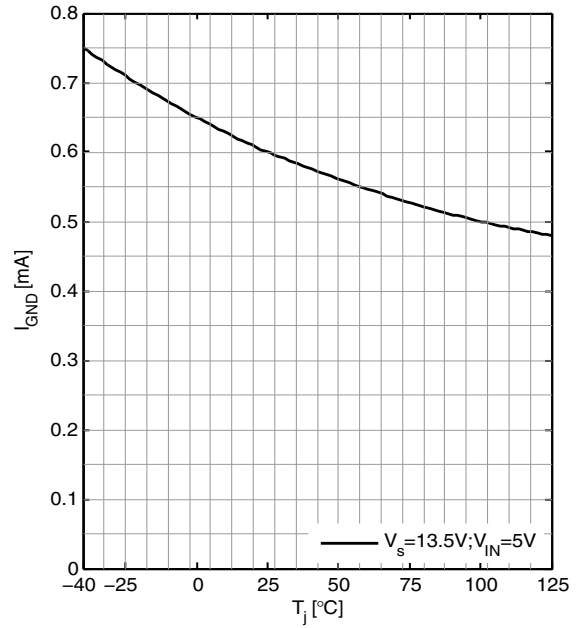


Typical Performance Characteristics

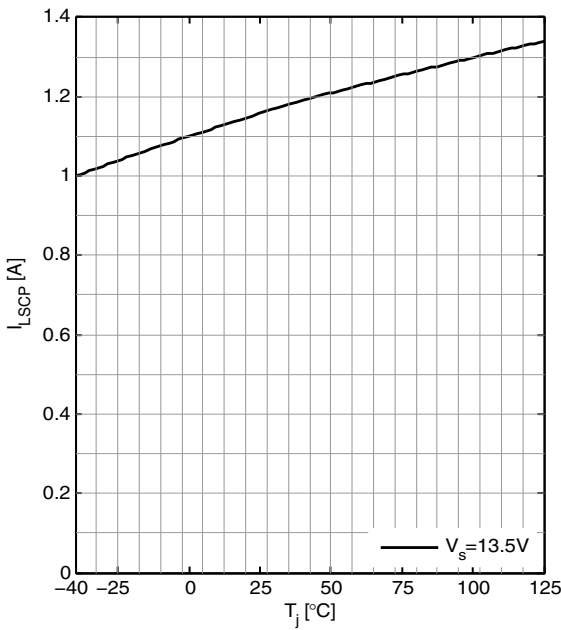
Standby Current I_{SSTB} versus Junction Temperature T_j



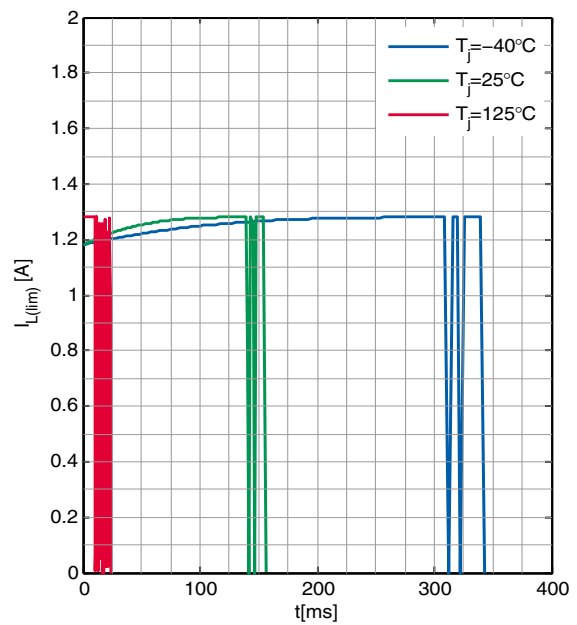
Operating Current I_{GND} versus Junction Temperature T_j



Initial Peak Short Circuit Current Limit I_{LSCP} versus Junction Temperature T_j

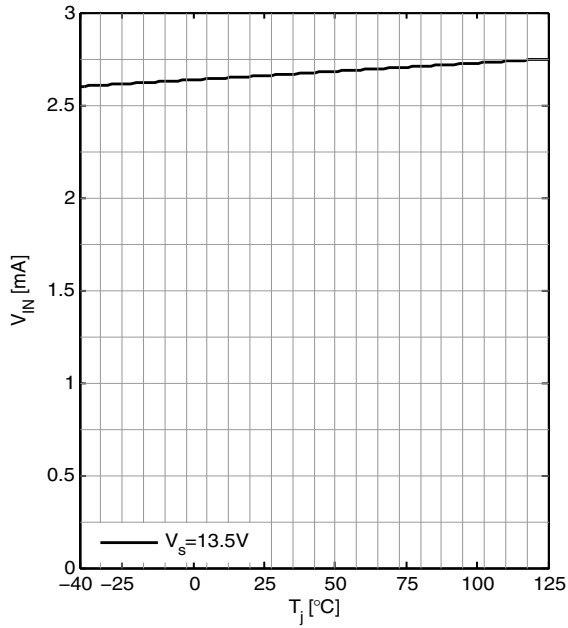


Typical Overload Current waveform; no heatsink; parameter: Start Temperature $T_{j-start}$

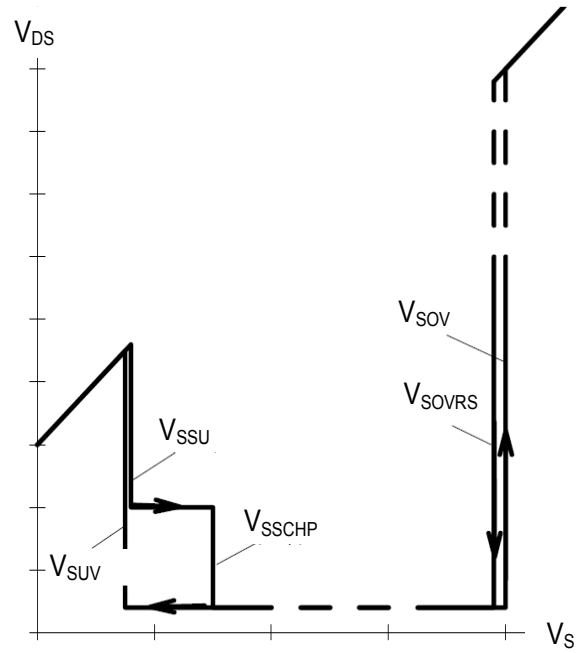


Typical Performance Characteristics

Input Threshold voltage $V_{INH,L}$ versus Junction Temperature T_j



Undervoltage restart of the charge pump



7 Application Information

7.1 Application Diagram

The following information is given as a hint for the implementation of the device only and shall not be regarded as a description or warranty for a certain functionality, condition or quality of the device.

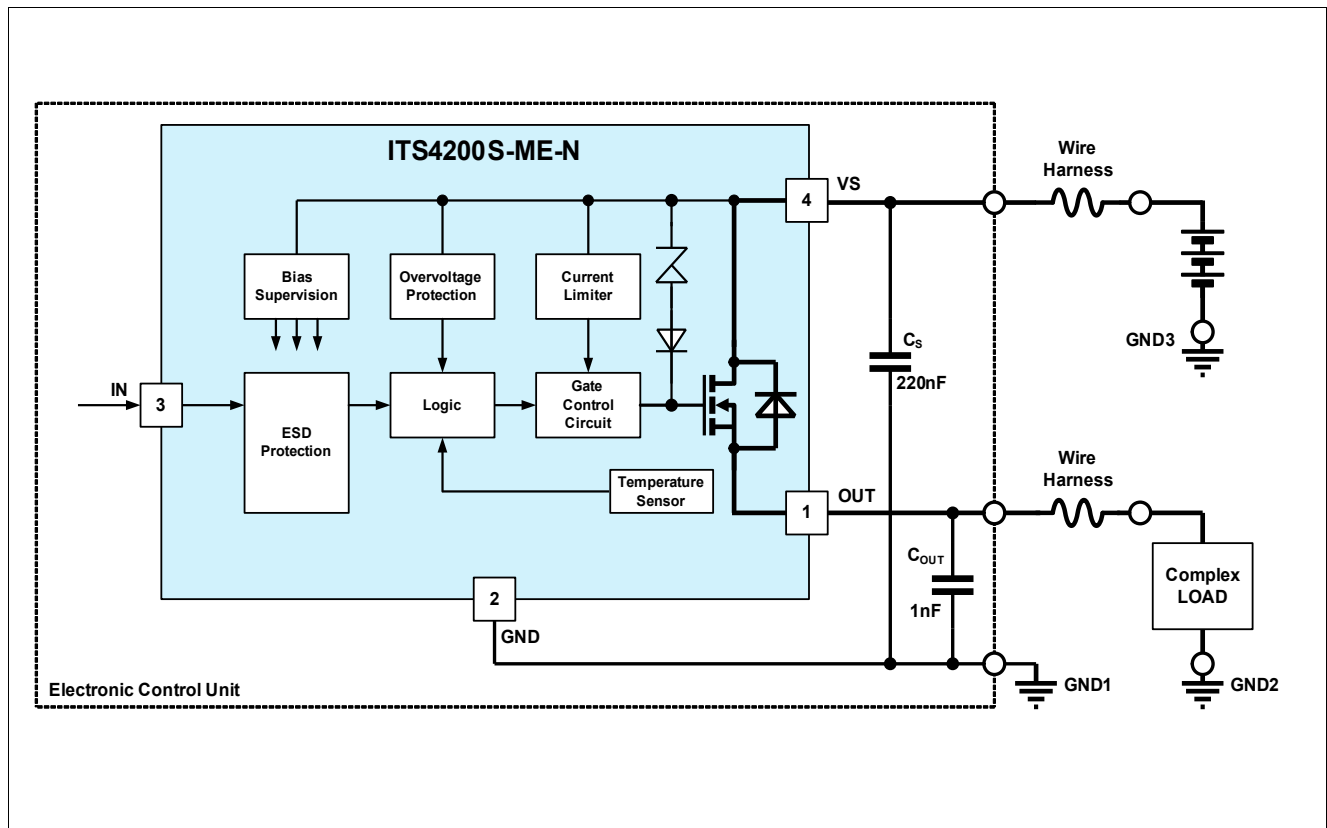


Figure 4 Application Diagram

The ITS4200S-ME-N can be connected directly to a supply network. It is recommended to place a ceramic capacitor (e.g. $C_S = 220\text{nF}$) between supply and GND to avoid line disturbances. Wire harness inductors/resistors are sketched in the application circuit above.

The complex load (resistive, capacitive or inductive) must be connected to the output pin OUT.

A built-in current limit protects the device against destruction.

The ITS4200S-ME-N can be switched on and off with standard logic ground related logic signal at pin IN.

In standby mode (IN=L) the ITS4200S-ME-N is deactivated with very low current consumption.

The output voltage slope is controlled during on and off transition to minimize emissions. Only a small ceramic capacitor $C_{OUT}=1\text{nF}$ is recommended to attenuate RF noise.

In the following chapters the main features, some typical waveforms and the protection behaviour of the **ITS4200S-ME-N** is shown. For further details please refer to application notes on the Infineon homepage.

7.2 Special Feature Description

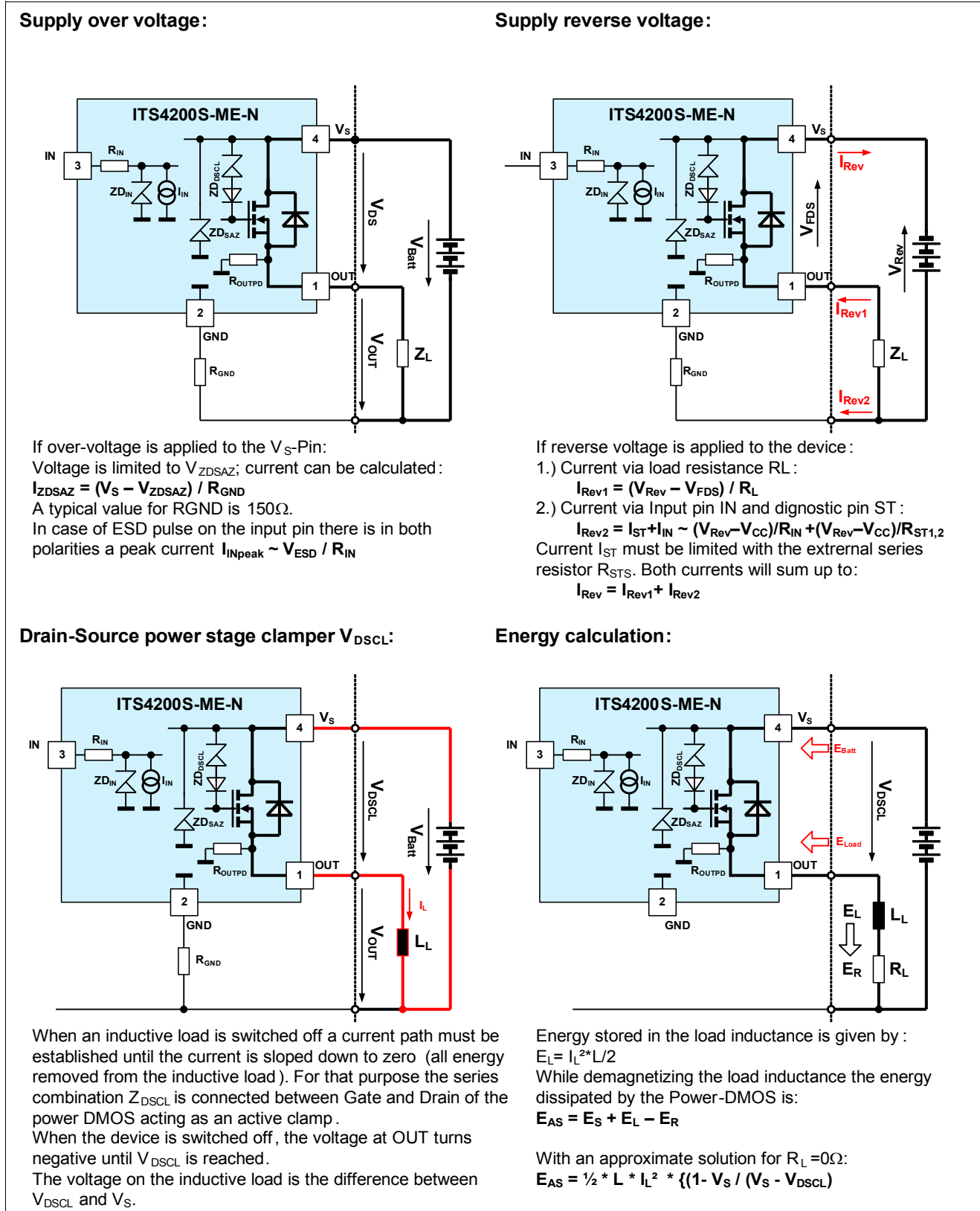


Figure 5 Special feature description

7.3 Typical Application Waveforms

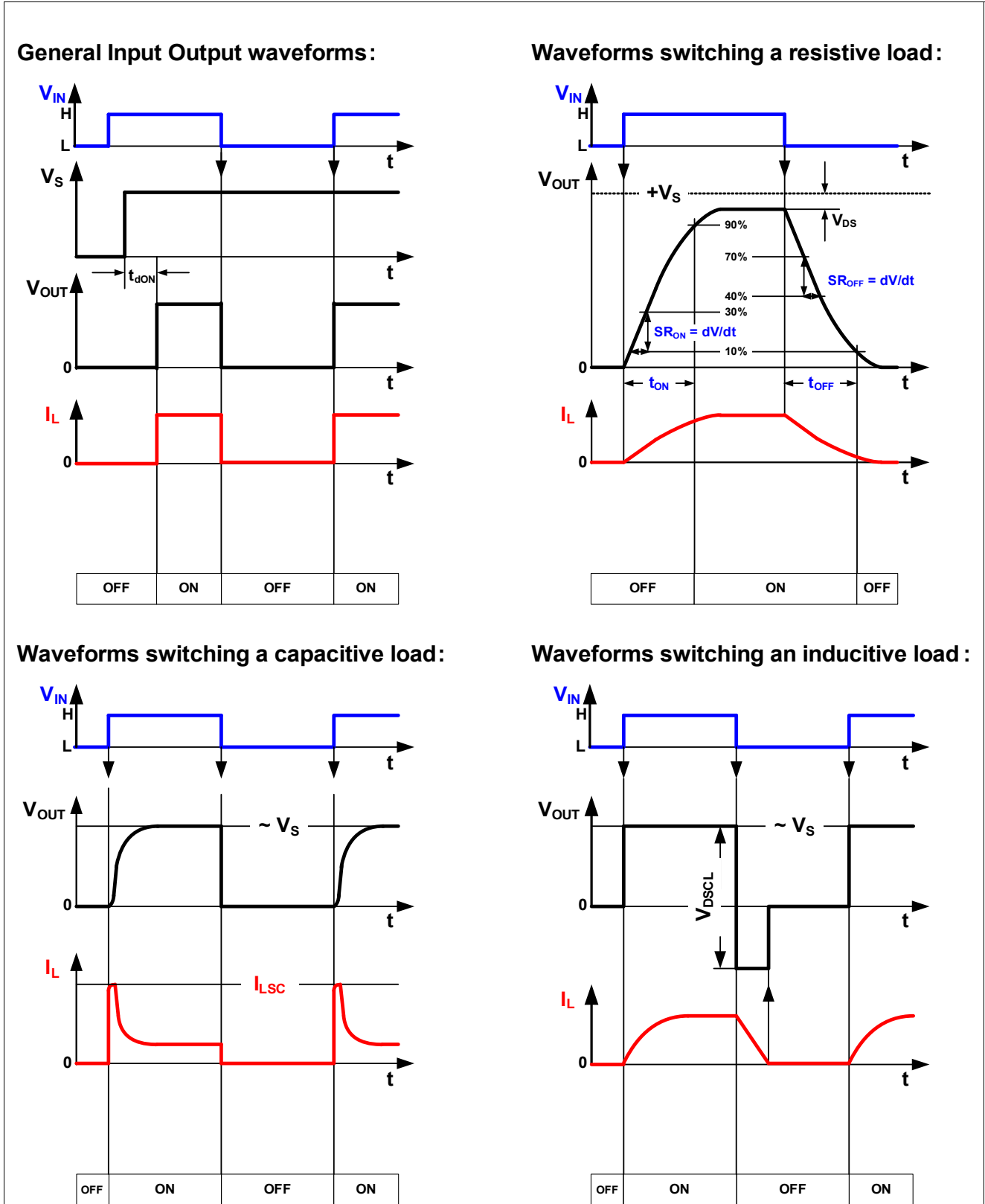


Figure 6 Typical application waveforms of the ITS4200S-ME-N

7.4 Protection Behavior

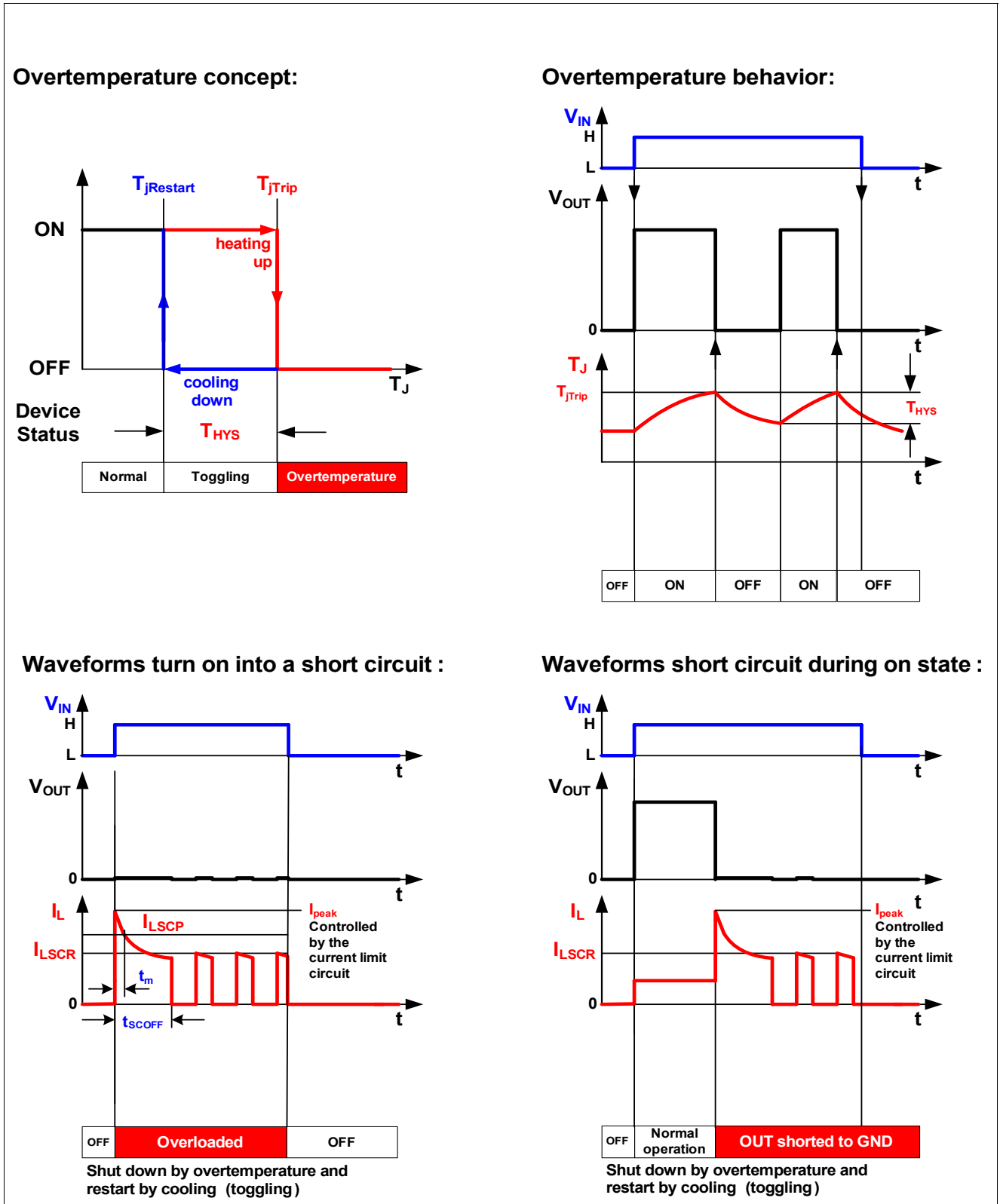


Figure 7 Protective behaviour of the ITS4200S-ME-N

8 Package outlines and footprint

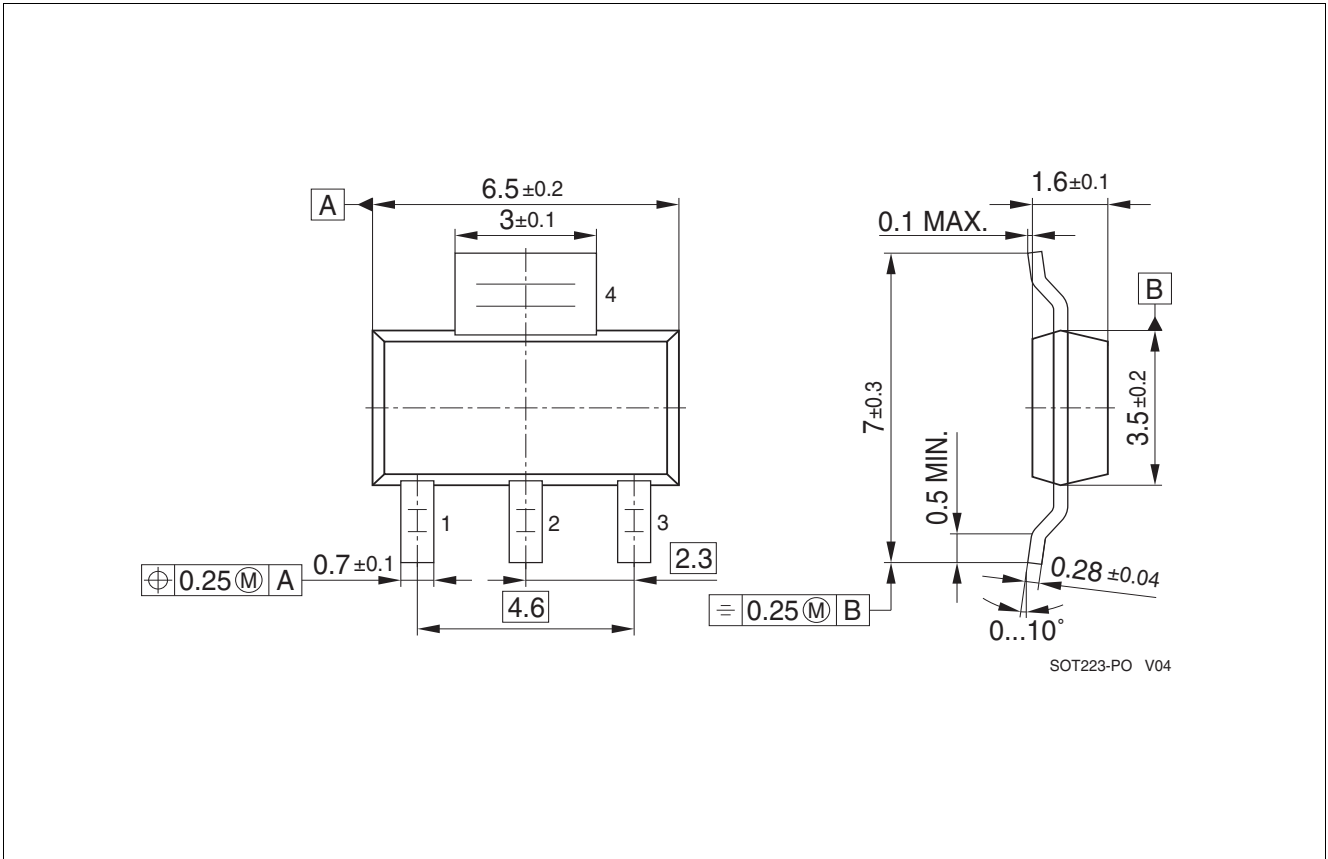


Figure 8 SOT-223-4 (Plastic Dual Small Outline Package, RoHS-Compliant)

To meet the world-wide customer requirements for environmentally friendly products and to be compliant with government regulations the device is available as a green product. Green products are RoHS-Compliant (i.e. Pb-free finish on leads and suitable for Pb-free soldering according to IPC/JEDEC J-STD-020)

9 Revision History

Revision	Date	Changes
1.0	2012-09-01	Datasheet release

Trademarks of Infineon Technologies AG

AURIX™, C166™, CanPAK™, CIPOS™, CIPURSE™, EconoPACK™, CoolMOS™, CoolSET™, CORECONTROL™, CROSSAVE™, DAVE™, DI-POL™, EasyPIM™, EconoBRIDGE™, EconoDUAL™, EconoPIM™, EconoPACK™, EiceDRIVER™, eupec™, FCOS™, HITFET™, HybridPACK™, I²RF™, ISOFACE™, IsoPACK™, MIPAQ™, ModSTACK™, my-d™, NovalithIC™, OptiMOS™, ORIGA™, POWERCODE™, PRIMARION™, PrimePACK™, PrimeSTACK™, PRO-SIL™, PROFET™, RASIC™, ReverSave™, SatRIC™, SIEGET™, SINDRION™, SIPMOS™, SmartLEWIS™, SOLID FLASH™, TEMPFET™, thinQ!™, TRENCHSTOP™, TriCore™.

Other Trademarks

Advance Design System™ (ADS) of Agilent Technologies, AMBA™, ARM™, MULTI-ICE™, KEIL™, PRIMECELL™, REALVIEW™, THUMB™, μVision™ of ARM Limited, UK. AUTOSAR™ is licensed by AUTOSAR development partnership. Bluetooth™ of Bluetooth SIG Inc. CAT-iq™ of DECT Forum. COLOSSUS™, FirstGPS™ of Trimble Navigation Ltd. EMV™ of EMVCo, LLC (Visa Holdings Inc.). EPCOS™ of Epcos AG. FLEXGO™ of Microsoft Corporation. FlexRay™ is licensed by FlexRay Consortium. HYPERTERMINAL™ of Hilgraeve Incorporated. IEC™ of Commission Electrotechnique Internationale. IrDA™ of Infrared Data Association Corporation. ISO™ of INTERNATIONAL ORGANIZATION FOR STANDARDIZATION. MATLAB™ of MathWorks, Inc. MAXIM™ of Maxim Integrated Products, Inc. MICROTEC™, NUCLEUS™ of Mentor Graphics Corporation. MIPI™ of MIPI Alliance, Inc. MIPS™ of MIPS Technologies, Inc., USA. muRata™ of MURATA MANUFACTURING CO., MICROWAVE OFFICE™ (MWO) of Applied Wave Research Inc., OmniVision™ of OmniVision Technologies, Inc. Openwave™ Openwave Systems Inc. RED HAT™ Red Hat, Inc. RFMD™ RF Micro Devices, Inc. SIRIUS™ of Sirius Satellite Radio Inc. SOLARIS™ of Sun Microsystems, Inc. SPANSION™ of Spansion LLC Ltd. Symbian™ of Symbian Software Limited. TAIYO YUDEN™ of Taiyo Yuden Co. TEAKLITE™ of CEVA, Inc. TEKTRONIX™ of Tektronix Inc. TOKO™ of TOKO KABUSHIKI KAISHA TA. UNIX™ of X/Open Company Limited. VERILOG™, PALLADIUM™ of Cadence Design Systems, Inc. VLYNQ™ of Texas Instruments Incorporated. VXWORKS™, WIND RIVER™ of WIND RIVER SYSTEMS, INC. ZETEX™ of Diodes Zetex Limited.

Last Trademarks Update 2011-11-11

Edition 2012-09-01

**Published by
Infineon Technologies AG
81726 Munich, Germany**

**© 2012 Infineon Technologies AG
All Rights Reserved.**

Legal Disclaimer

The information given in this document shall in no event be regarded as a guarantee of conditions or characteristics. With respect to any examples or hints given herein, any typical values stated herein and/or any information regarding the application of the device, Infineon Technologies hereby disclaims any and all warranties and liabilities of any kind, including without limitation, warranties of non-infringement of intellectual property rights of any third party.

Information

For further information on technology, delivery terms and conditions and prices, please contact the nearest Infineon Technologies Office (www.infineon.com).

Warnings

Due to technical requirements, components may contain dangerous substances. For information on the types in question, please contact the nearest Infineon Technologies Office.

The Infineon Technologies component described in this Data Sheet may be used in life-support devices or systems and/or automotive, aviation and aerospace applications or systems only with the express written approval of Infineon Technologies, if a failure of such components can reasonably be expected to cause the failure of that life-support automotive, aviation and aerospace device or system or to affect the safety or effectiveness of that device or system. Life support devices or systems are intended to be implanted in the human body or to support and/or maintain and sustain and/or protect human life. If they fail, it is reasonable to assume that the health of the user or other persons may be endangered.