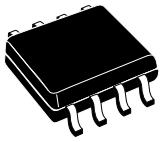
# STGAP2S

## Galvanically isolated 4 A single gate driver

**Datasheet - production data**



SO-8

## Features

- 1700 V single channel gate driver
- Driver current capability: 4 A sink / source at 25 °C
- dV/dt transient immunity ± 100 V/ns
- Overall input-output propagation delay: 80 ns
- Separate sink and source for easy gate driving configuration
- 4 A Miller clamp dedicated pin
- UVLO function
- Gate driving voltage up to 26 V
- 3.3 V, 5 V TTL/CMOS inputs with hysteresis
- Temperature shutdown protection
- Standby function

## Applications

- Motor driver for home appliances, factory automation, industrial drives and fans.
- 600/1200 V inverters
- Battery chargers
- Induction heating
- Welding
- UPS
- Power supply units
- DC-DC converters
- Power factor correction

## Description

The STGAP2S is a single gate driver which isolates the gate driving channel from the low voltage control and interface circuitry.

The gate driver is characterized by 4 A capability and rail-to-rail outputs, making the device also suitable for high power inverter applications such as motor drivers in industrial applications.

The device is available in two different configurations. The configuration with separated output pins allows to independently optimize turn-on and turn-off by using dedicated gate resistors. A configuration featuring single output pin and Miller clamp function prevents gate spikes during fast commutations in half-bridge topologies.

Both configurations provide high flexibility and bill of material reduction for external components.

The device integrates protection functions: UVLO and thermal shutdown are included to easily design high reliability systems. Dual input pins allow choosing the control signal polarity and also implementing HW interlocking protection in order to avoid cross-conduction in case of controller malfunction.

The input to output propagation delay results contained within 80 ns, providing high PWM control accuracy.

A standby mode is available in order to reduce idle power consumption.



This is information on a product in full production. www.st.com

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# 1 Block diagram

**Figure 1. Block diagram - separated outputs option**

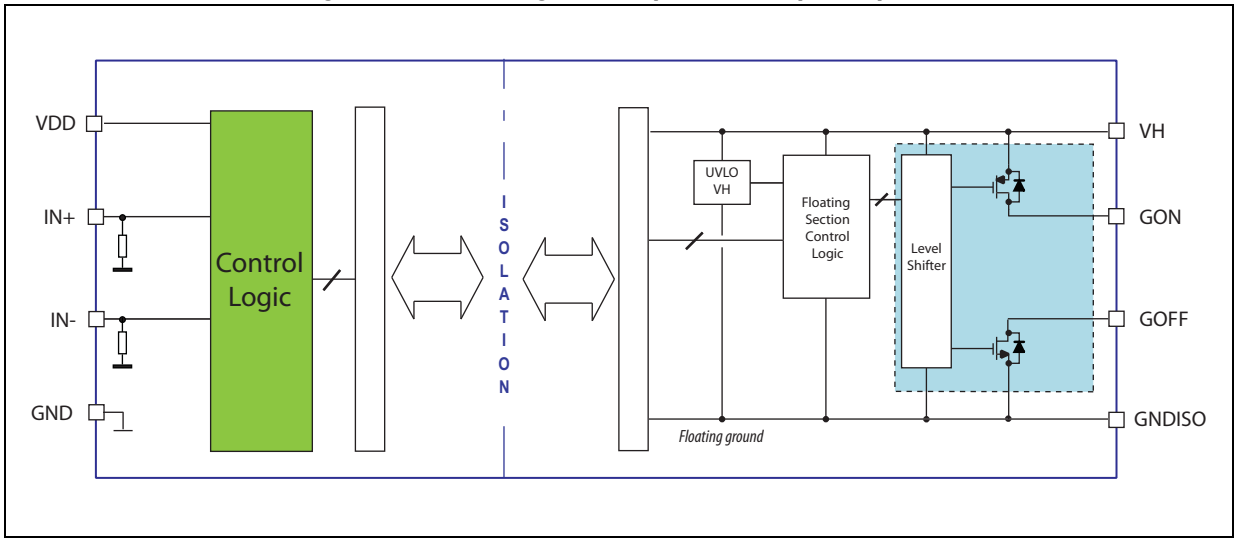
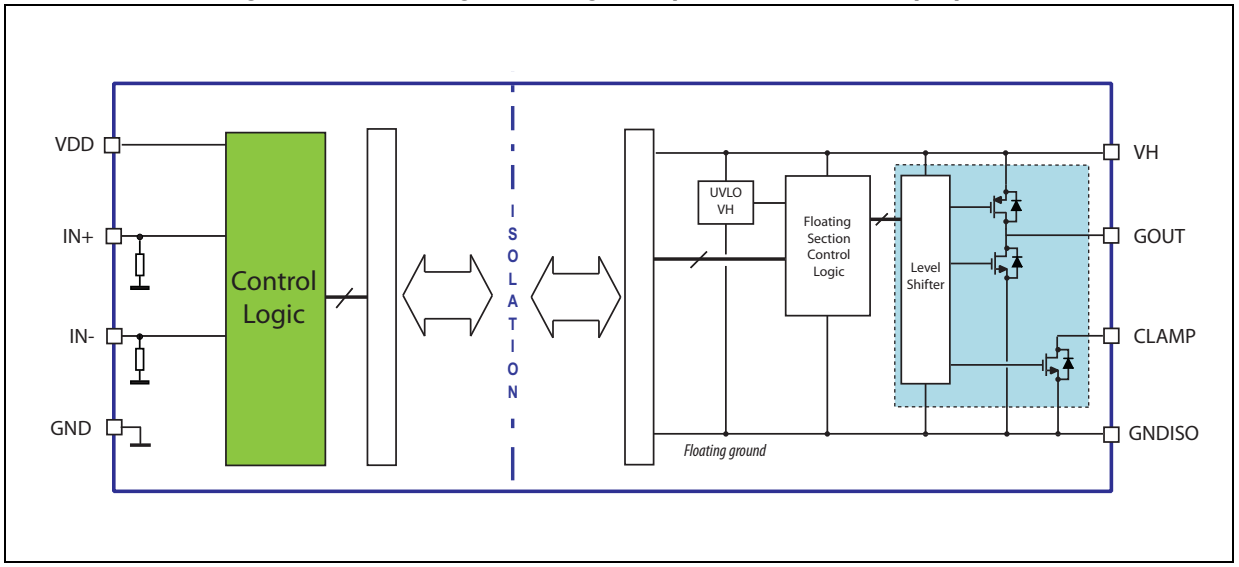



**Figure 2. Block diagram - single output and Miller clamp option**



# 2 Pin description and connection diagram

**Figure 3. Pin connection (top view), separated outputs option**

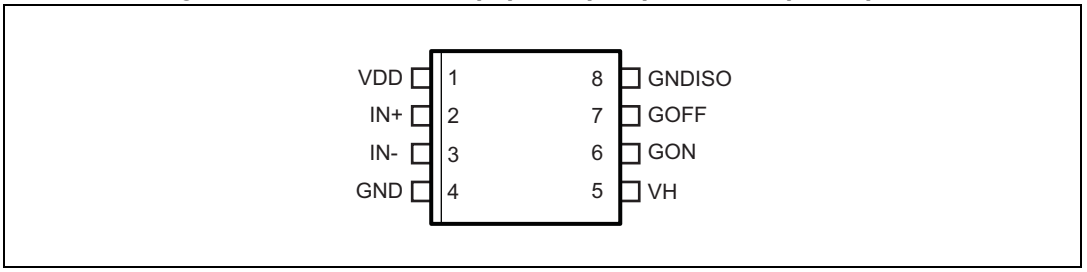



**Figure 4. Pin connection (top view), single output and Miller clamp option**

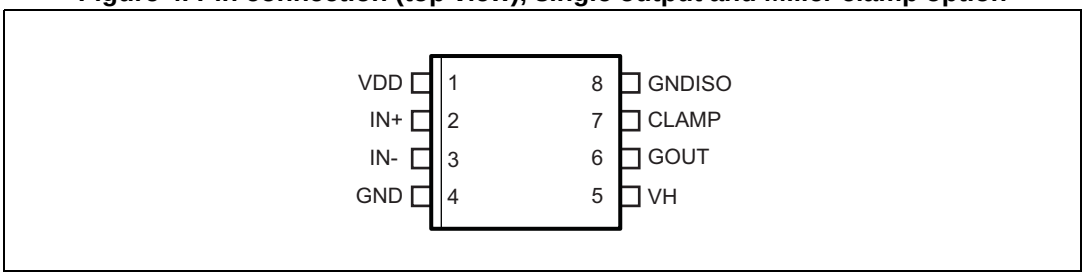



**Table 1. Pin description**

| Pin no. | | Pin name | Type | Function |
|---|---|---|---|---|
| *Figure 3* | *Figure 4* | | | |
| 1 | 1 | VDD | Power supply | Driver logic supply voltage. |
| 2 | 2 | IN+ | Logic input | Driver logic input, active high. |
| 3 | 3 | $\overline{\text{IN-}}$ | Logic input | Driver logic input, active low. |
| 4 | 4 | GND | Power supply | Driver logic ground. |
| 5 | 5 | VH | Power supply | Gate driving positive voltage supply. |
| - | 6 | GOUT | Analog output | Sink/source output. |
| - | 7 | CLAMP | Analog output | Active Miller clamp. |
| 6 | - | GON | Analog output | Source output. |
| 7 | - | GOFF | Analog output | Sink output. |
| 8 | 8 | GNDISO | Power supply | Gate driving Isolated ground. |

# 3 Electrical data

## 3.1 Absolute maximum ratings

**Table 2. Absolute maximum ratings**

| Symbol | Parameter | Test condition | Min. | Max. | Unit |
|---|---|---|---|---|---|
| VDD | Logic supply voltage vs. GND | - | -0.3 | 6.5 | V |
| $V_{LOGIC}$ | Logic pins voltage vs. GND | - | -0.3 | 6.5 | V |
| VH | Positive supply voltage (VH vs. GNDISO) | - | -0.3 | 28 | V |
| $V_{OUT}$ | Voltage on gate driver outputs (GON, GOFF, CLAMP vs. GNDISO) | - | - 0.3 | VH + 0.3 | V |
| $V_{iso}$ | Input to output isolation voltage (GND vs. GNDISO) | DC or peak | -1700 | +1700 | V |
| $T_J$ | Junction temperature | - | -40 | 150 | °C |
| $T_S$ | Storage temperature | - | -50 | 150 | °C |
| $P_{Din}$ | Power dissipation input chip | $T_A$ = 25 °C | - | 10 | mW |
| $P_{Dout}$ | Power dissipation output chip | $T_A$ = 25 °C | - | 850 | mW |
| ESD | HBM (human body model) | - | 2 | | kV |

## 3.2 Thermal data

**Table 3. Thermal data**

| Symbol | Parameter | Package | Value | Unit |
|---|---|---|---|---|
| $R_{th(JA)}$ | Thermal resistance junction to ambient | SO-8 | 130 | °C/W |

## 3.3 Recommended operating conditions

**Table 4. Recommended operating conditions**

| Symbol | Parameter | Test conditions | Min. | Max. | Unit |
|---|---|---|---|---|---|
| VDD | Logic supply voltage vs. GND | - | 3 | 5.5 | V |
| $V_{LOGIC}$ | Logic pins voltage vs. GND | - | 0 | 5.5 | V |
| VH | Positive supply voltage (VH vs. GNDISO) | - | - | 26 | V |
| $f_{SW}$ | Maximum switching frequency(1) | - | - | 4 | MHz |
| $T_{IN}$ | Pulse width at IN+, IN- | - | 100 | - | ns |
| $T_J$ | Operating junction temperature | - | -40 | 125 | °C |

1. Actual limit depends on power dissipation and $T_J$.

# 4 Electrical characteristics

**Table 5. Electrical characteristics**
**($T_J$ = 25 °C, VH = 15 V, VDD = 5 V, unless otherwise specified)**

| Symbol | Pin | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|
| **Dynamic characteristics** | | | | | | | |
| $t_{Don}$ | IN+, IN- | Input to output propagation delay ON | - | - | 80 | 100 | ns |
| $t_{Doff}$ | IN+, IN- | Input to output propagation delay OFF | - | - | 80 | 100 | ns |
| $t_r$ | - | Rise time | $C_L$ = 4.7 nF, 10% ÷ 90% | - | 30 | - | ns |
| $t_f$ | - | Fall time | $C_L$ = 4.7 nF, 90% ÷ 10% | - | 30 | - | ns |
| PWD | - | Pulse width distortion $\lvert t_{Don} - t_{Doff} \rvert$ | - | - | - | 20 | ns |
| $t_{deglitch}$ | IN+, IN- | Inputs deglitch filter | - | - | 20 | 40 | ns |
| CMTI(1) | - | Common-mode transient immunity, $\lvert dV_{ISO}/dt \rvert$ | $V_{CM}$ = 1500 V, see *Figure 14 on page 16* | 100 | - | - | V/ns |
| **Supply voltage** | | | | | | | |
| $VH_{on}$ | - | VH UVLO turn-on threshold | - | 8 | 9.1 | 10.5 | V |
| $VH_{off}$ | - | VH UVLO turn-off threshold | - | 7 | 8.4 | 9.5 | V |
| $VH_{hyst}$ | - | VH UVLO hysteresis | - | 0.5 | 0.9 | 1.4 | V |
| $I_{QHU}$ | - | VH undervoltage quiescent supply current | VH = 4 V | - | 150 | 250 | µA |
| $I_{QH}$ | - | VH quiescent supply current | - | - | 1.3 | 2.5 | mA |
| $I_{QHSBY}$ | - | Standby VH quiescent supply current | Standby mode | - | 400 | 600 | µA |
| SafeClp | - | GOFF active clamp | $I_{GOFF}$ = 0.2 A; VH floating | - | 2 | 2.5 | V |
| $I_{QDD}$ | - | VDD quiescent supply current | - | - | 0.5 | 0.8 | mA |
| $I_{QDDSBY}$ | - | Standby VDD quiescent supply current | Standby mode | - | 40 | 80 | µA |
| **Logic inputs** | | | | | | | |
| $V_{il}$ | IN+, IN- | Low level logic threshold voltage | - | 0.29 · VDD | 1/3 · VDD | 0.37 · VDD | V |
| $V_{ih}$ | IN+, IN- | High level logic threshold voltage | - | 0.62 · VDD | 2/3 · VDD | 0.72 · VDD | V |

**Table 5. Electrical characteristics**
**($T_J$ = 25 °C, VH = 15 V, VDD = 5 V, unless otherwise specified) (continued)**

| Symbol | Pin | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|
| $I_{INh}$ | IN+, IN- | INx logic “1” input bias current | INx = 5 V | 33 | 50 | 77 | µA |
| $I_{INl}$ | IN+, IN- | INx logic “0” input bias current | INx = GND | - | - | 1 | µA |
| $R_{pd}$ | IN+, IN- | Inputs pull-down resistors | INx = 5 V | 65 | 100 | 150 | kΩ |
| **Driver buffer section** | | | | | | | |
| $I_{GON}$ | - | Source short-circuit current | $T_J$ = 25 °C | - | 4 | - | A |
| | | | $T_J$ = -40 ÷ +125 °C(1) | 3 | - | 5 | |
| $V_{GONH}$ | - | Source output high level voltage | $I_{GON}$ = 100 mA | VH -0.14 | VH -0.11 | - | V |
| $R_{GON}$ | - | Source $R_{DS_ON}$ | $I_{GON}$ = 100 mA | - | 1.11 | 1.4 | Ω |
| $I_{GOFF}$ | - | Sink short-circuit current | $T_J$ = 25 °C | - | 4 | - | A |
| | | | $T_J$ = -40 ÷ +125 °C(1) | 3 | - | 5.5 | |
| $V_{GOFFL}$ | - | Sink output low level voltage | $I_{GOFF}$ = 100 mA | - | 84 | 95 | mV |
| $R_{GOFF}$ | - | Sink $R_{DS_ON}$ | $I_{GOFF}$ = 100 mA | - | 0.84 | 0.95 | Ω |
| **Miller Clamp function (STGAP2SC only)** | | | | | | | |
| $V_{CLAMPth}$ | - | CLAMP voltage threshold | $V_{CLAMP}$ vs. GNDISO | 1.3 | 2 | 2.6 | V |
| $I_{CLAMP}$ | - | CLAMP short-circuit current | $V_{CLAMP}$ = 15 V | - | | | A |
| | | | $T_J$ = 25 °C | - | 4 | - | |
| | | | $T_J$ = -40 ÷ +125 °C(1) | 2 | - | 5 | |
| $V_{CLAMP_L}$ | - | CLAMP low level output voltage | $I_{CLAMP}$ = 100 mA | - | 89 | 100 | mV |
| $R_{CLAMP}$ | - | CLAMP $R_{DS_ON}$ | $I_{CLAMP}$ = 100 mA | - | 0.89 | 1.00 | Ω |
| **Overtemperature protection** | | | | | | | |
| $T_{SD}$ | - | Shutdown temperature | - | 170 | - | - | °C |
| $T_{hys}$ | - | Temperature hysteresis | - | - | 20 | - | °C |
| **Standby** | | | | | | | |
| $t_{STBY}$ | - | Standby time | See *Section 5.3* | 200 | 280 | 350 | µs |
| $t_{WUP}$ | - | Wake-up time | See *Section 5.3* | 10 | 20 | 35 | µs |
| $t_{awake}$ | - | Wake-up delay | See *Section 5.3* | 90 | 140 | 200 | µs |
| $t_{stbyfilt}$ | - | Standby filter | See *Section 5.3* | 200 | 280 | 600 | ns |

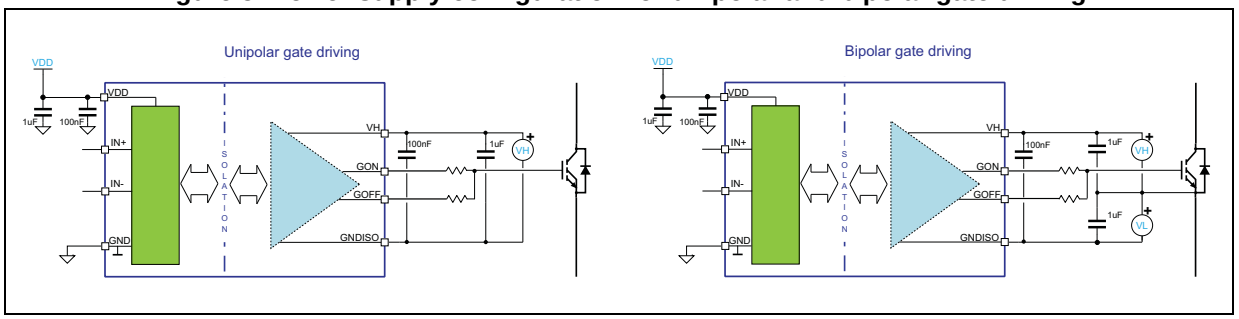
1. Characterization data, not tested in production.

# 5 Functional description

## 5.1 Gate driving power supply and UVLO

The STGAP2S is a flexible and compact gate driver with 4 A output current and rail-to-rail outputs. The device allows implementation of either unipolar or bipolar gate driving.

**Figure 5. Power supply configuration for unipolar and bipolar gate driving**




Undervoltage protection is available on VH supply pin. A fixed hysteresis sets the turn-off threshold, thus avoiding intermittent operation.

When VH voltage goes below the $VH_{off}$ threshold, the output buffer goes in “safe state”. When VH voltage reaches the $VH_{on}$ threshold, the device returns to normal operation and sets the output according to actual input pins status.

The VDD and VH supply pins must be properly filtered with local bypass capacitors. The use of capacitors with different values in parallel provides both local storage for impulsive current supply and high-frequency filtering. The best filtering is obtained by using low-ESR SMT ceramic capacitors, which are therefore recommended. A 100 nF ceramic capacitor must be placed as close as possible to each supply pin, and a second bypass capacitor with value in the range between 1 µF and 10 µF should be placed close to it.

## 5.2 Power up, power down and 'safe state'

The following conditions define the “safe state”:

- GOFF = ON state
- GON = high impedance
- CLAMP = ON state (for STGAP2SC)

Such conditions are maintained at power up of the isolated side ($VH < VH_{on}$) and during whole device power down phase ($VH < VH_{off}$), regardless of the value of the input pins.

The device integrates a structure which clamps the driver output to a voltage not higher than SafeClp when VH voltage is not high enough to actively turn the internal GOFF MOSFET on. If VH positive supply pin is floating or not supplied the GOFF pin is therefore clamped to a voltage smaller than SafeClp.

If the supply voltage VDD of the control section of the device is not supplied, the output is put in *safe state*, and remains in such condition until the VDD voltage returns within operative conditions.

After power-up of both isolated and low voltage side the device output state depends on the input pins' status.

## 5.3 Control inputs

The device is controlled through the IN+ and IN- logic inputs, in accordance to the truth table described in *Table 6*.

**Table 6. Inputs truth table (applicable when device is not in UVLO or "safe state")**

| Input pins | | Output pins | |
|---|---|---|---|
| **IN+** | **IN-** | **GON** | **GOFF** |
| L | L | OFF | ON |
| H | L | **ON** | **OFF** |
| L | H | OFF | ON |
| H | H | OFF | ON |

A deglitch filter allow the input pins to ignore signals with duration shorter than $t_{deglitch}$, so preventing noise spikes possibly present in the application from generating unwanted commutations.

## 5.4 Miller clamp function

The Miller clamp function allows the control of the Miller current during the power stage switching in half-bridge configurations. When the external power transistor is in the OFF state, the driver operates to avoid the induced turn-on phenomenon that may occur when the other switch in the same leg is being turned on, due to the $C_{GD}$ capacitance.

During the turn-off period the gate of the external switch is monitored through the CLAMP pin. The CLAMP switch is activated when gate voltage goes below the voltage threshold. $V_{CLAMPth}$, thus creating a low impedance path between the switch gate and the GNDISO pin.

## 5.5 Watchdog

The isolated HV side has a watchdog function in order to identify when it is not able to communicate with LV side, for example because the VDD of the LV side is not supplied. In this case the output of the driver is forced in "safe state" until communication link is properly established again.

## 5.6 Thermal shutdown protection

The device provides a thermal shutdown protection. When junction temperature reaches the $T_{SD}$ temperature threshold, the device is forced in "safe state". The device operation is restored as soon as the junction temperature is lower than $T_{SD}$ - $T_{hys}$.

## 5.7 Standby function

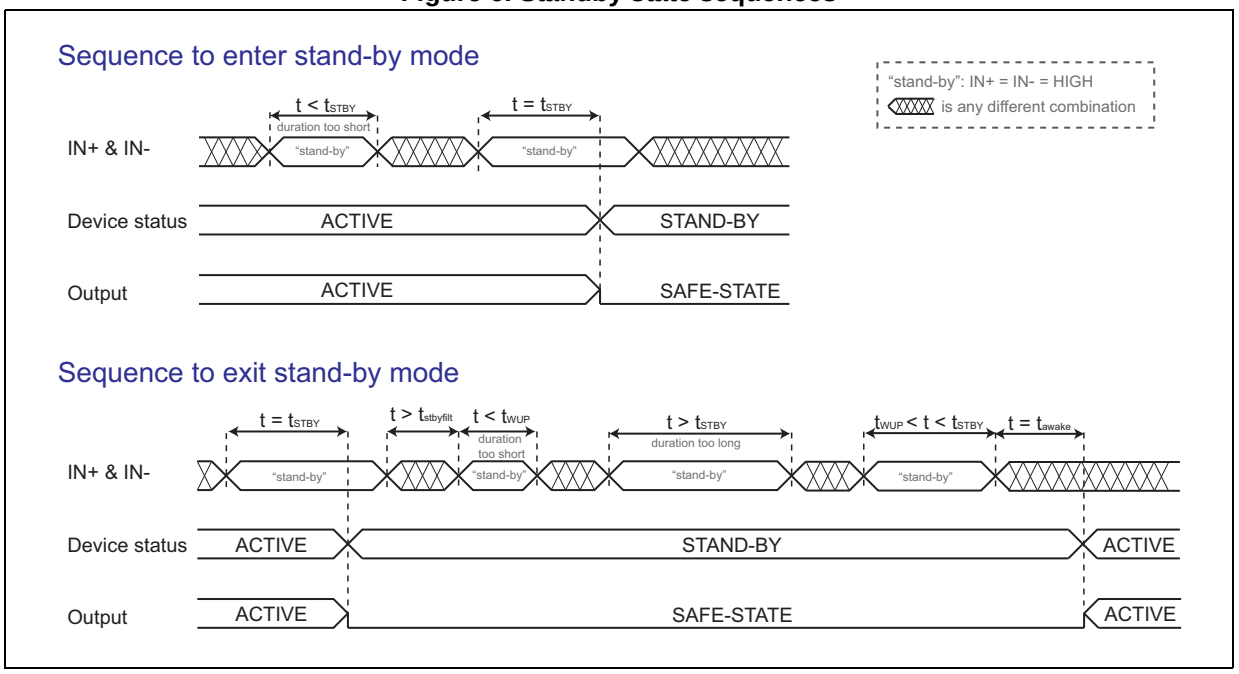
In order to reduce the power consumption of both control interface and gate driving sides the device can be put in standby mode. In standby mode the quiescent current from VDD and VH supply pins is reduced to $I_{QDDSBY}$ and $I_{QHSBY}$ respectively, and the output remains in 'safe state' (the output is actively forced low).

The way to enter standby is to keep both IN+ and IN- high (“standby” value) for a time longer than $t_{STBY}$. During standby the inputs can change from the “stand-by” value.

To exit stand-by, IN+ and IN- must be put in any combination different from the “standby” value for a time longer than $t_{stbyfilt}$ , and then in the “standby” value for a time t such that $t_{WUP} < t < t_{STBY}$.

When the input configuration is changed from the “standby” value the output is enabled and set according to inputs state after a time $t_{awake}$.

**Figure 6. Standby state sequences**



# 6 Typical application diagram

**Figure 7. Typical application diagram - separated outputs**

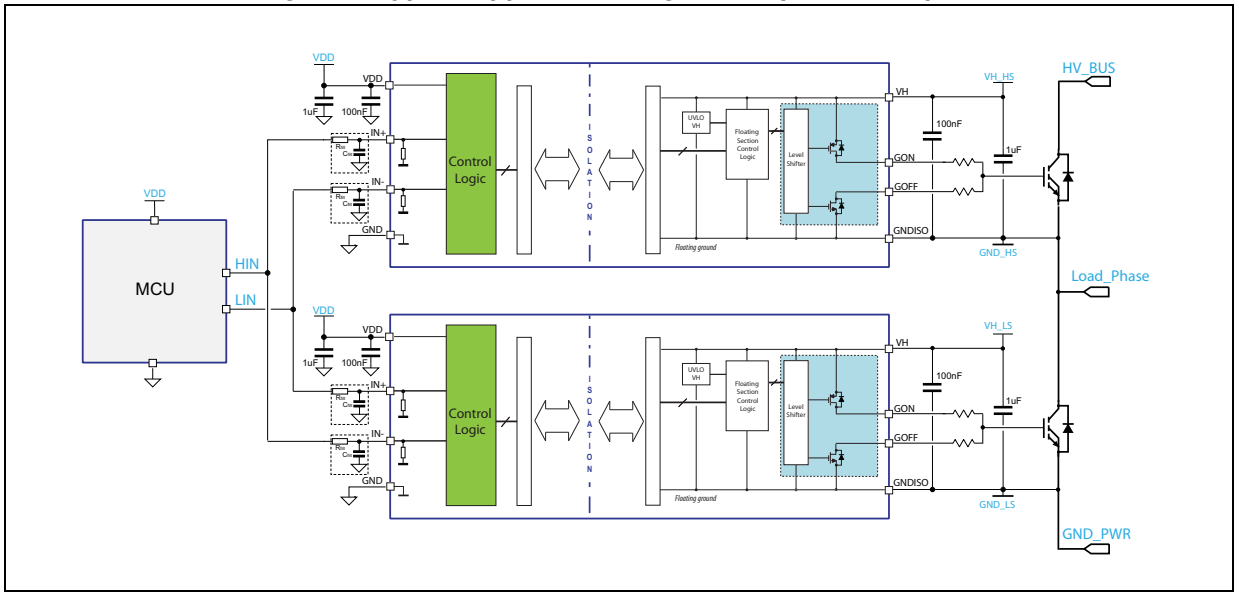



**Figure 8. Typical application diagram - separated outputs and negative gate driving**

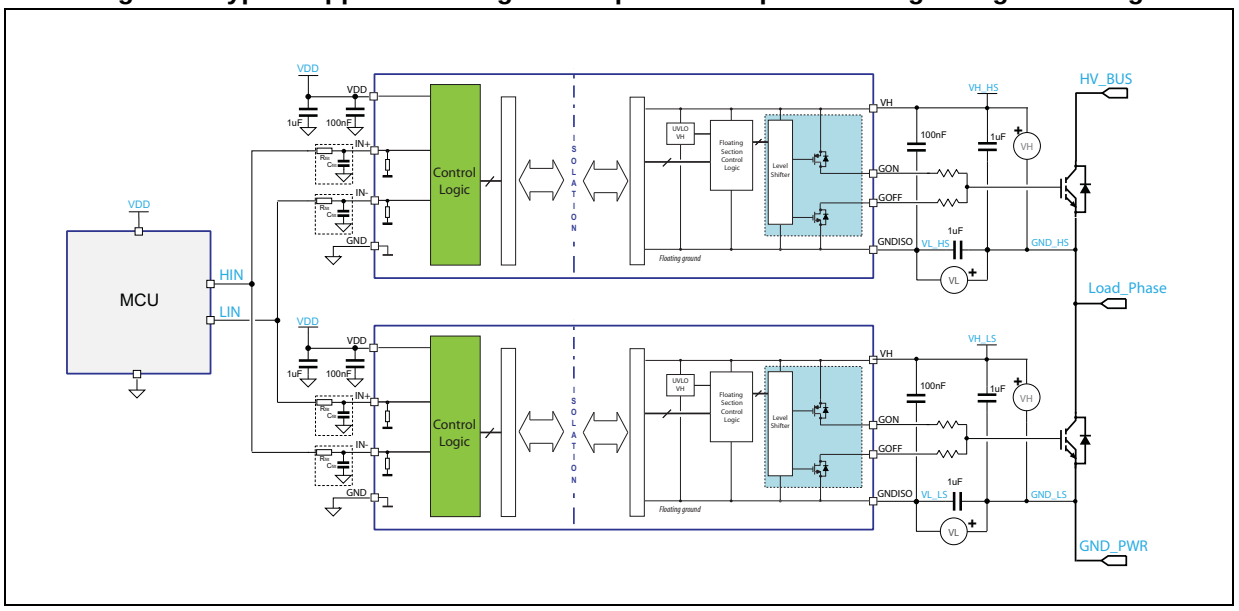


**Figure 9. Typical application diagram - Miller clamp**

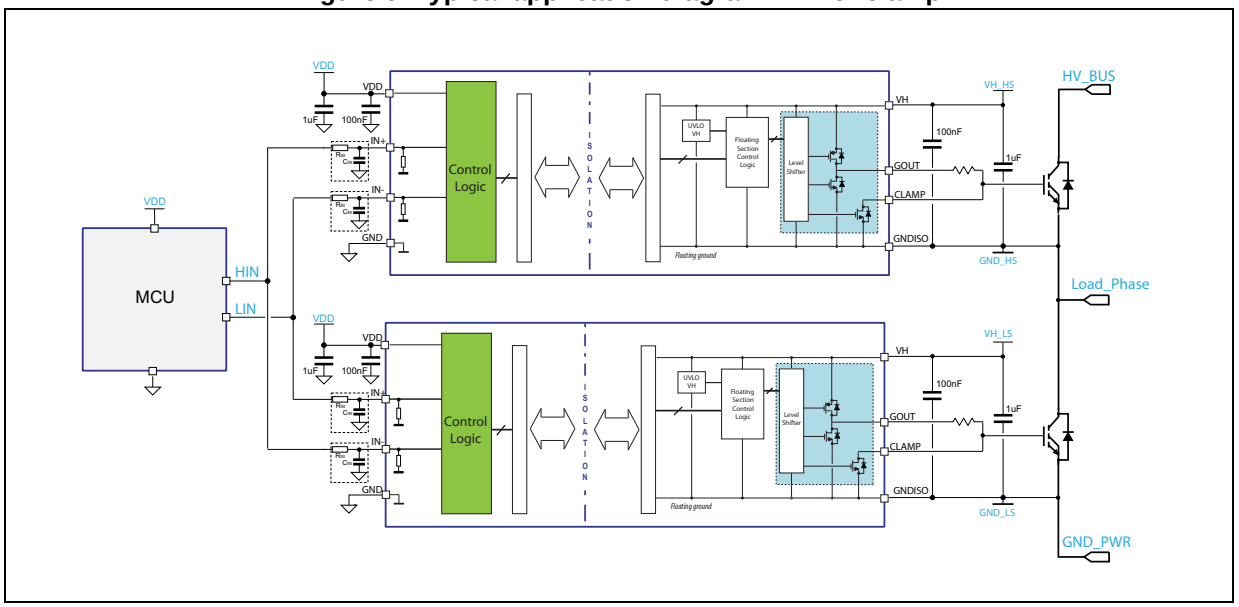
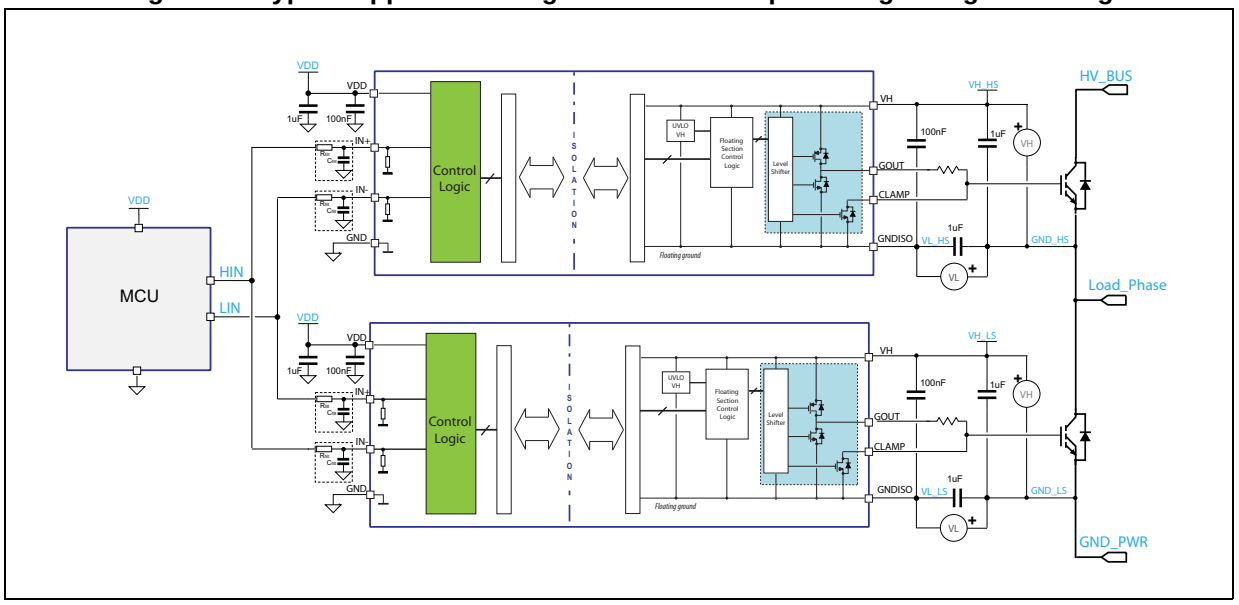



**Figure 10. Typical application diagram - Miller clamp and negative gate driving**



# 7 Layout

## 7.1 Layout guidelines and considerations

In order to optimize the PCB layout, following considerations should be taken into account:

- SMT ceramic capacitors (or different types of low-ESR and low-ESL capacitors) must be placed close to each supply rail pins. A 100 nF capacitor must be placed between VDD and GND and between VH and GNDISO, as close as possible to device pins, in order to filter high-frequency noise and spikes. In order to provide local storage for pulsed current a second capacitor with value in the range between 1 µF and 10 µF should also be placed close to the supply pins.
- As a good practice it is suggested to add filtering capacitors close to logic inputs of the device (IN+, IN-), in particular for fast switching or noisy applications.
- The power transistors must be placed as close as possible to the gate driver, so to minimize the gate loop area and inductance that might bring to noise or ringing.
- To avoid degradation of the isolation between the primary and secondary side of the driver, there should not be any trace or conductive area below the driver.
- If the system has multiple layers, it is recommended to connect the VH and GNDISO pins to internal ground or power planes through multiple vias of adequate size. These vias should be located close to the IC pins to maximize thermal conductivity.

## 7.2 Layout example

An example of STGAP2SC Half-Bridge PCB layout with main signals highlighted by different colors is shown in *Figure 11* and *Figure 12*. It is recommended to follow this example for proper positioning and connection of filtering capacitors.

**Figure 11. Top layer traces and copper**

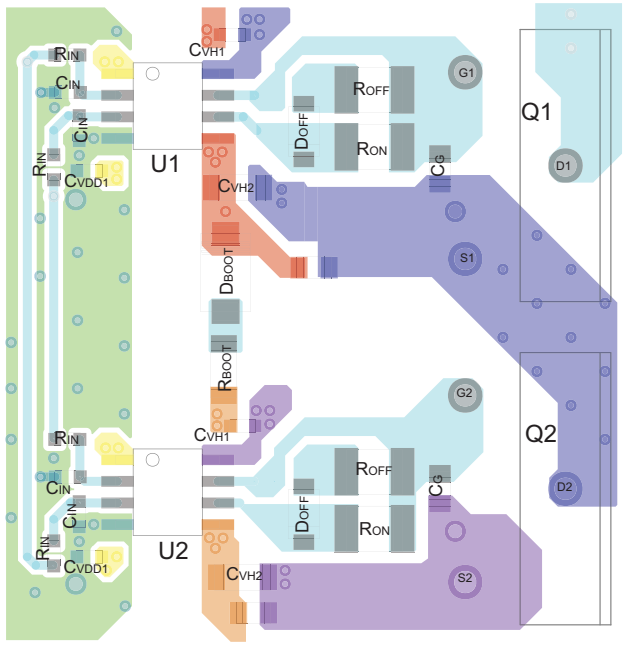
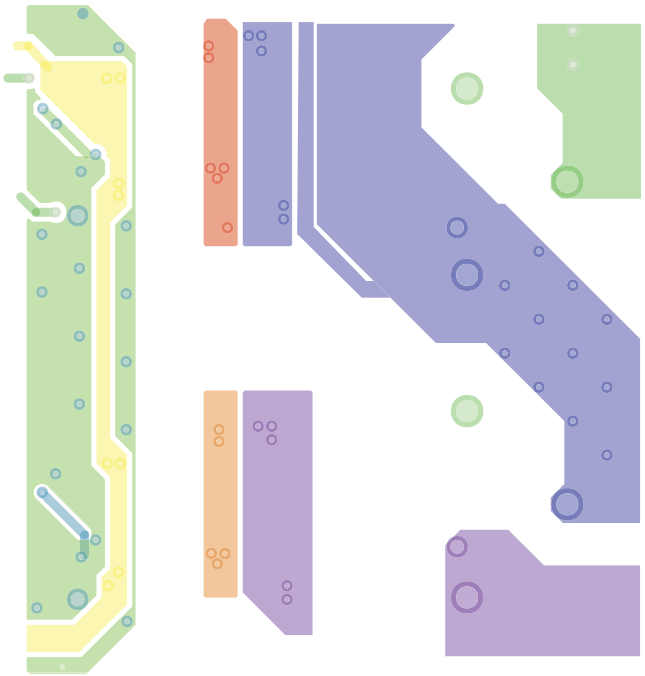



**Figure 12. Bottom layer traces and copper**



# 8 Testing and characterization information

**Figure 13. Timings definition**

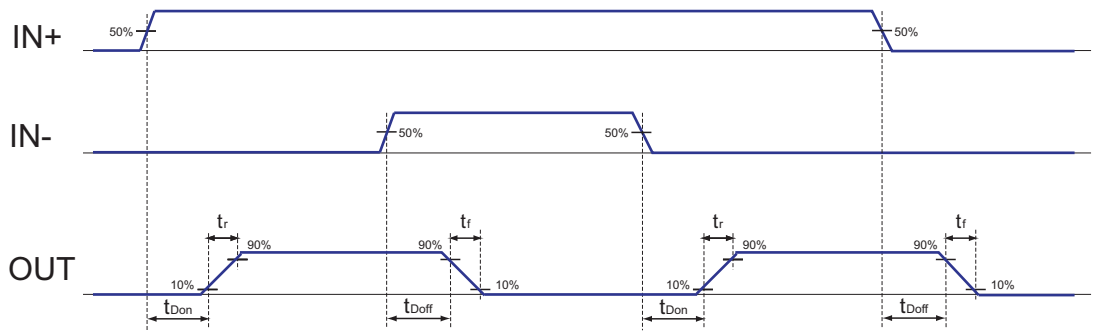
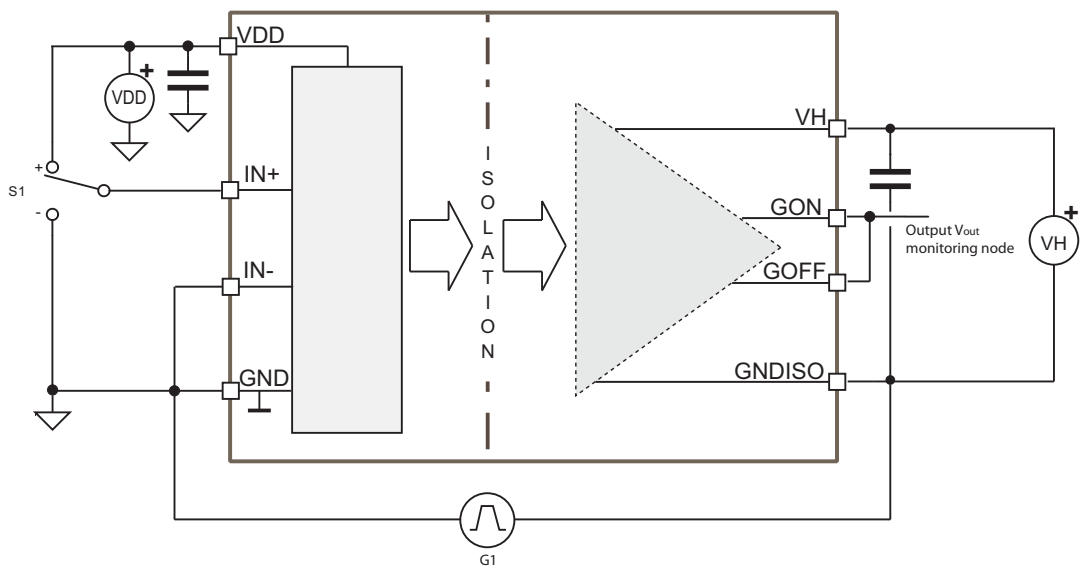



**Figure 14. CMTI test circuit**



# 9 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

## 9.1 SO-8 package information

**Figure 15. SO-8 package outline**

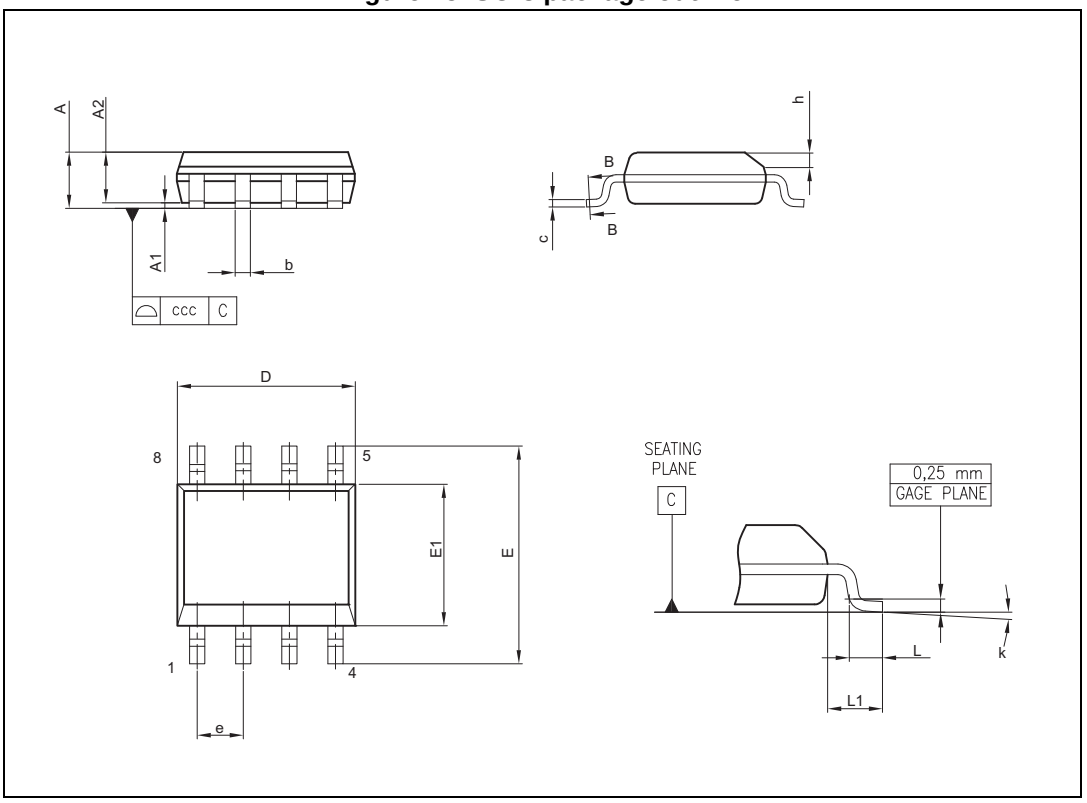
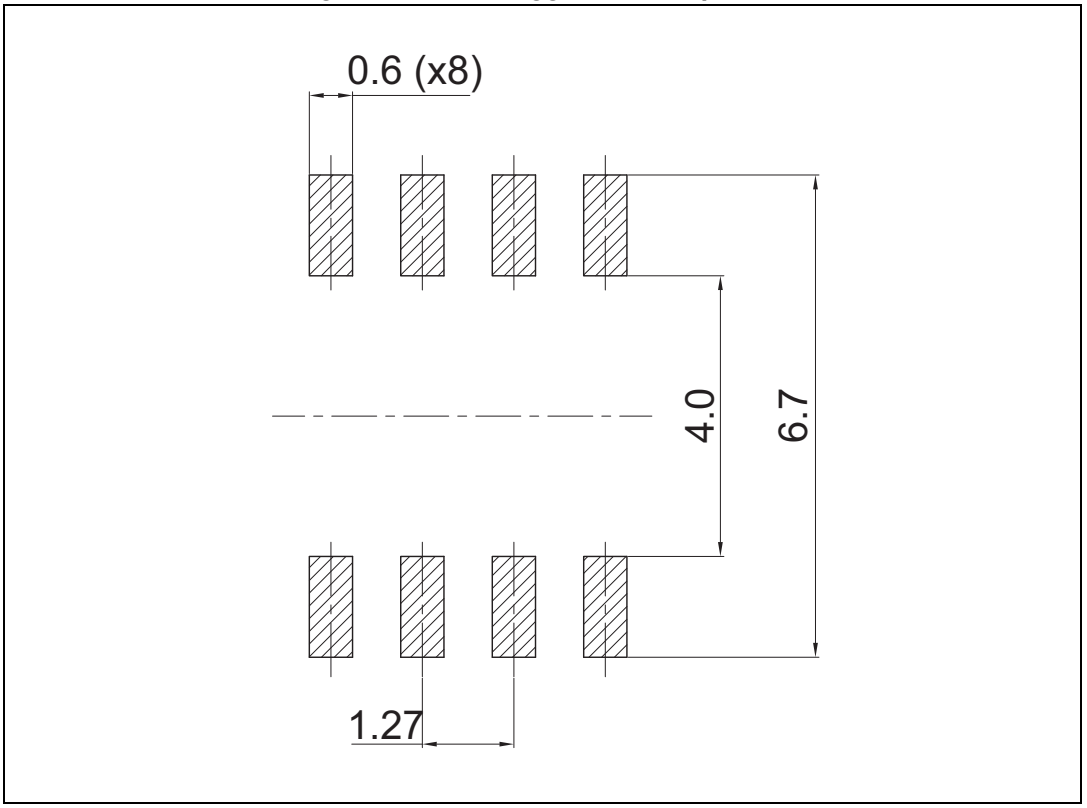



**Table 7. SO-8 package mechanical data**

| Symbol | Dimensions (mm) | | | Notes |
|---|---|---|---|---|
| | Min. | Typ. | Max. | |
| A | - | - | 1.75 | - |
| A1 | 0.10 | - | 0.25 | - |
| A2 | 1.25 | - | - | - |
| b | 0.28 | - | 0.48 | - |
| c | 0.17 | - | 0.23 | - |
| D | 4.80 | 4.90 | 5.00 | - |
| E | 5.80 | 6.00 | 6.20 | - |
| E1 | 3.80 | 3.90 | 4.00 | - |
| e | - | 1.27 | - | - |
| h | 0.25 | - | 0.50 | - |
| L | 0.40 | - | 1.27 | - |
| L1 | - | 1.04 | - | - |
| k | 0 | - | 8 | Degrees |
| ccc | - | - | 0.10 | - |

# 10 Suggested land pattern

**Figure 16. SO-8 suggested land pattern**



# 11 Ordering information

**Table 8. Device summary**

| Order code | Output configuration | Package marking | Package | Packaging |
|---|---|---|---|---|
| STGAP2SM | GON-GOFF | GAP2S2 | SO-8 | Tube |
| STGAP2SMTR | GON-GOFF | GAP2S2 | SO-8 | Tape and reel |
| STGAP2SCM | GOUT-CLAMP | GAP2SC2 | SO-8 | Tube |
| STGAP2SCMTR | GOUT-CLAMP | GAP2SC2 | SO-8 | Tape and reel |

# 12 Revision history

**Table 9. Document revision history**

| Date | Revision | Changes |
|---|---|---|
| 06-Jun-2018 | 1 | Initial release. |

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