1. DESCRIPTION

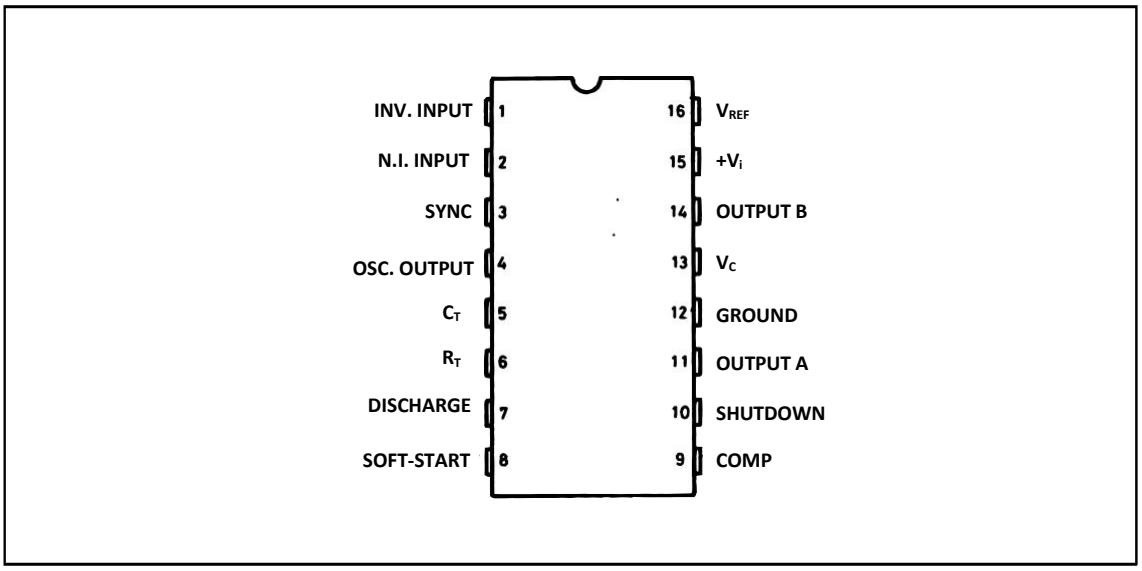
The XL3525 series of pulse width modulator integrated circuits are designed to offer improved performance and lowered external parts count when used in designing all types of switching power supplies. The on-chip + 5.1 V reference is trimmed to ± 1 % and the input common mode range of the error amplifier includes the reference voltage eliminating external resistors. A sync input to the oscillator allows multiple units to be slaved or a single unit to be synchronized to an external system clock. A single resistor between the CT and the discharge terminals provide a wide range of dead time adjustment.

These devices also feature built in soft-start circuitry with only an external timing capacitor required. A shutdown terminal controls both the soft-start circuity and the output stages, providing instantaneous turn off through the PWM latch with pulsed shutdown, as well as soft-start recycle with longer shutdown commands. These functions are also controlled by an undervoltage lockout which keeps the outputs off and the soft-start capacitor discharged for subnormal input voltages. This lockout circuitry includes approximately 500 mV of hysteresis for jitterfree operation. Another feature of these PWM circuits is a latch following the comparator. Once a PWM pulses has been terminated for any reason, the outputs will remain off for the duration of the period. The latch is reset with each clock pulse. The output stages are totempole designs capable of sourcing or sinking in excess of 200 mA. The XL3525K output stage features NOR logic, giving a LOW output for an OFF state.

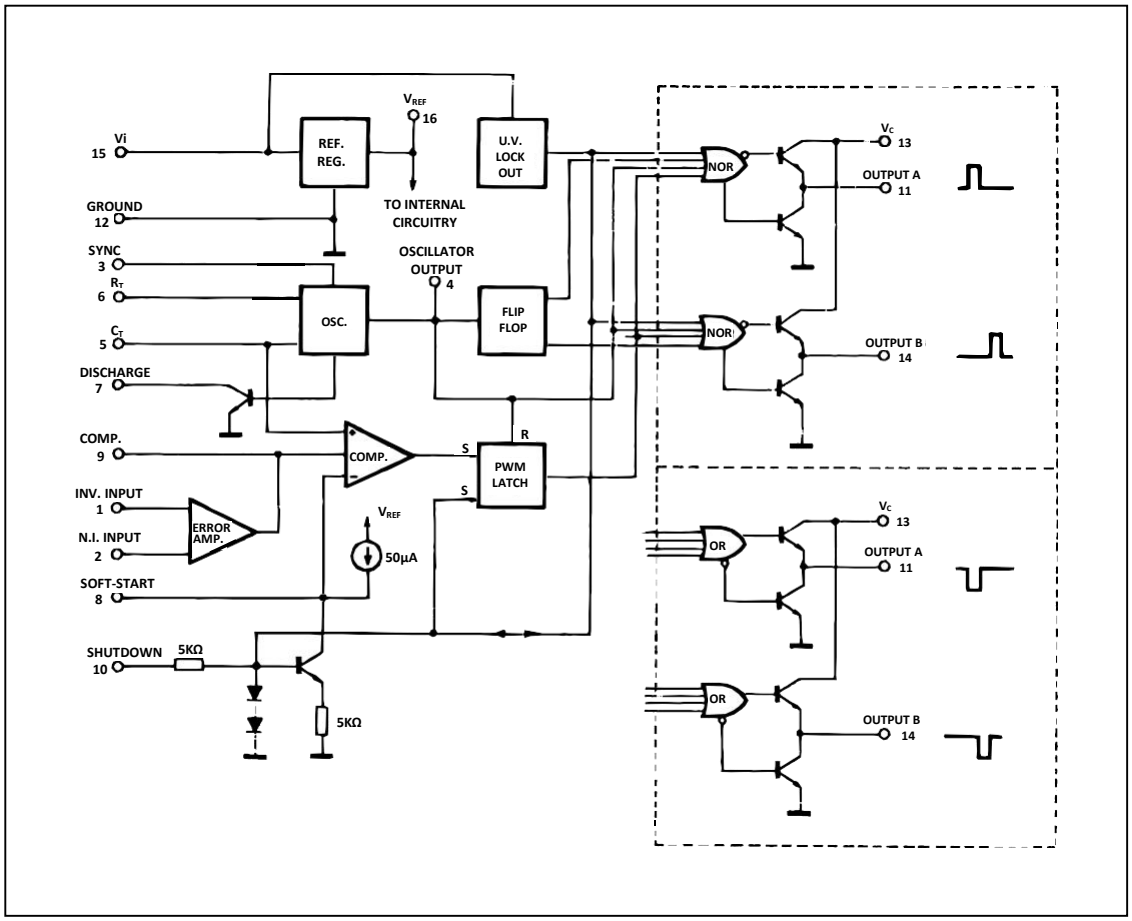
2. FEATURES

- 8 TO 35 V OPERATION
- 5.1 V REFERENCE TRIMMED TO ± 1 %
- 100 Hz TO 500 KHz OSCILLATOR RANGE
- SEPARATE OSCILLATOR SYNC TERMINAL
- ADJUSTABLE DEADTIME CONTROL
- PULSE-BY-PULSE SHUTDOWN
- INPUT UNDERVOLTAGE LOCKOUT WITH HYSTERESIS
- LATCHING PWM TO PREVENT MULTIPLE PULSES
- DUAL SOURCE/SINK OUTPUT DRIVERS

3. PIN CONNECTIONS



4. FUNCTIONAL BLOCK DIAGRAM



Block Diagram

5. SPECIFICATIONS

5.1. Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
V_i	Supply Voltage	40	V
V_C	Collector Supply Voltage	40	V
I_{OSC}	Oscillator Charging Current	5	mA
I_o	Output Current, Source or Sink	500	mA
I_R	Reference Output Current	50	mA
I_T	Current through C_T Terminal Logic Inputs Analog Inputs	5 – 0.3 to + 5.5 – 0.3 to V_i	mA V V
P_{tot}	Total Power Dissipation at T_{amb} = 70 °C	1000	mW
T_j	Junction Temperature Range	– 55 to 150	°C
T_{stg}	Storage Temperature Range	– 65 to 150	°C
T_{op}	Operating Ambient Temperature : **XL2525K** **XL3525K**	– 25 to 85 0 to 70	°C °C

5.2. Thermal Resistance Characteristics

Symbol	Parameter	SO16	DIP16	Unit
$R_{th\ j\text{-}pins}$	Thermal Resistance Junction-pins		50	°C/W
$R_{th\ j\text{-}amb}$	Thermal Resistance Junction-ambient		80	°C/W
$R_{th\ j\text{-}alumina}$	Thermal Resistance Junction-alumina (*)	50		°C/W

[1] Thermal resistance junction-alumina with the device soldered on the middle of an alumina supporting substrate measuring 15 × 20 mm ; 0.65 mm thickness with infinite heatsink.

5.3. Recommended Operating Conditions

Parameter	Value
Input Voltage (V_i)	8 to 35 V
Collector Supply Voltage (V_C)	4.5 to 35 V
Sink/Source Load Current (steady state)	0 to 100 mA
Sink/Source Load Current (peak)	0 to 400 mA
Reference Load Current	0 to 20 mA
Oscillator Frequency Range	100 Hz to 400 KHz
Oscillator Timing Resistor	2 KΩ to 150 KΩ
Oscillator Timing Capacitor	0.001 µF to 0.1 µF
Dead Time Resistor Range	0 to 500 Ω

[1] Range over which the device is functional and parameter limits are guaranteed.

5.4. Electrical Characteristics

(V = 20 V, and over operating temperature, unless otherwise specified)

Symbol	Parameter	Test Conditions	XL2525K			XL3525K			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
REFERENCE SECTION									
V_{REF}	Output Voltage	T_j = 25 °C	5.05	5.1	5.15	5	5.1	5.2	V
ΔV_{REF}	Line Regulation	V_i = 8 to 35 V		10	20		10	20	mV
ΔV_{REF}	Load Regulation	I_L = 0 to 20 mA		20	50		20	50	mV
$\Delta V_{REF}/\Delta T$*	Temp. Stability	Over Operating Range		20	50		20	50	mV
*	Total Output Variation	Line, Load and Temperature	5		5.2	4.95		5.25	V
	Short Circuit Current	V_{REF} = 0 T_j = 25 °C		80	100		80	100	mA
*	Output Noise Voltage	10 Hz ≤f ≤ 10 kHz, T_j = 25 °C		40	200		40	200	μVrms
ΔV_{REF}*	Long Term Stability	T_j = 125 °C, 1000 hrs		20	50		20	50	mV
OSCILLATOR SECTION * *									
*, •	Initial Accuracy	T_j = 25 °C		± 2	± 6		± 2	± 6	%
*, •	Voltage Stability	V_i = 8 to 35 V		± 0.3	± 1		± 1	± 2	%
$\Delta f/\Delta T$*	Temperature Stability	Over Operating Range		± 3	± 6		± 3	± 6	%
f_{MIN}	Minimum Frequency	R_T = 200 KΩ C_T = 0.1 μF			120			120	Hz
f_{MAX}	Maximum Frequency	R_T = 2 KΩ C_T = 470 pF	400			400			KHz
	Current Mirror	I_{RT} = 2 mA	1.7	2	2.2	1.7	2	2.2	mA
*, •	Clock Amplitude		3	3.5		3	3.5		V
*, •	Clock Width	T_j = 25 °C	0.3	0.5	1	0.3	0.5	1	μs
	Sync Threshold		1.2	2	2.8	1.2	2	2.8	V
	Sync Input Current	Sync Voltage = 3.5 V		1	2.5		1	2.5	mA
ERROR AMPLIFIER SECTION (V_{CM} = 5.1 V)									
V_{OS}	Input Offset Voltage			0.5	5		2	10	mV
I_b	Input Bias Current			1	10		1	10	μA
I_{os}	Input Offset Current				1			1	μA
	DC Open Loop Gain	R_L ≥ 10 MΩ	60	75		60	75		dB
*	Gain Bandwidth Product	G_v = 0 dB T_j = 25 °C	1	2		1	2		MHz
*, ▮	DC Transconduct.	30 KΩ ≤ R_L ≤ 1 MΩ T_j = 25 °C	1.1	1.5		1.1	1.5		ms
	Output Low Level			0.2	0.5		0.2	0.5	V
	Output High Level		3.8	5.6		3.8	5.6		V
CMR	Comm. Mode Reject.	V_{CM} = 1.5 to 5.2 V	60	75		60	75		dB
PSR	Supply Voltage Rejection	V_i = 8 to 35 V	50	60		50	60		dB

ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Test Conditions	XL2525K			XL3525K			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
PWM COMPARATOR									
	Minimum Duty-cycle				0			0	%
•	Maximum Duty-cycle		45	49		45	49		%
•	Input Threshold	Zero Duty-cycle	0.7	0.9		0.7	0.9		V
		Maximum Duty-cycle		3.3	3.6		3.3	3.6	V
*	Input Bias Current			0.05	1		0.05	1	µA
SHUTDOWN SECTION									
	Soft Start Current	V_{SD} = 0 V, V_{SS} = 0 V	25	50	80	25	50	80	µA
	Soft Start Low Level	V_{SD} = 2.5 V		0.4	0.7		0.4	0.7	V
	Shutdown Threshold	To outputs, V_{SS} = 5.1 V T_j = 25 °C	0.6	0.8	1	0.6	0.8	1	V
	Shutdown Input Current	V_{SD} = 2.5 V		0.4	1		0.4	1	mA
*	Shutdown Delay	V_{SD} = 2.5 V T_j = 25 °C		0.2	0.5		0.2	0.5	µs
OUTPUT DRIVERS (each output) (V_C = 20 V)									
	Output Low Level	I_{sink} = 20 mA		0.2	0.4		0.2	0.4	V
		I_{sink} = 100 mA		1	2		1	2	V
	Output High Level	I_{source} = 20 mA	18	19		18	19		V
		I_{source} = 100 mA	17	18		17	18		V
	Under-Voltage Lockout	V_{comp} and V_{ss} = High	6	7	8	6	7	8	V
I_C	Collector Leakage	V_C = 35 V			200			200	µA
t_r*	Rise Time	C_L = 1 nF, T_j = 25 °C		100	600		100	600	ns
t_f*	Fall Time	C_L = 1 nF, T_j = 25 °C		50	300		50	300	ns
TOTAL STANDBY CURRENT									
I_s	Supply Current	V_i = 35 V		14	20		14	20	mA

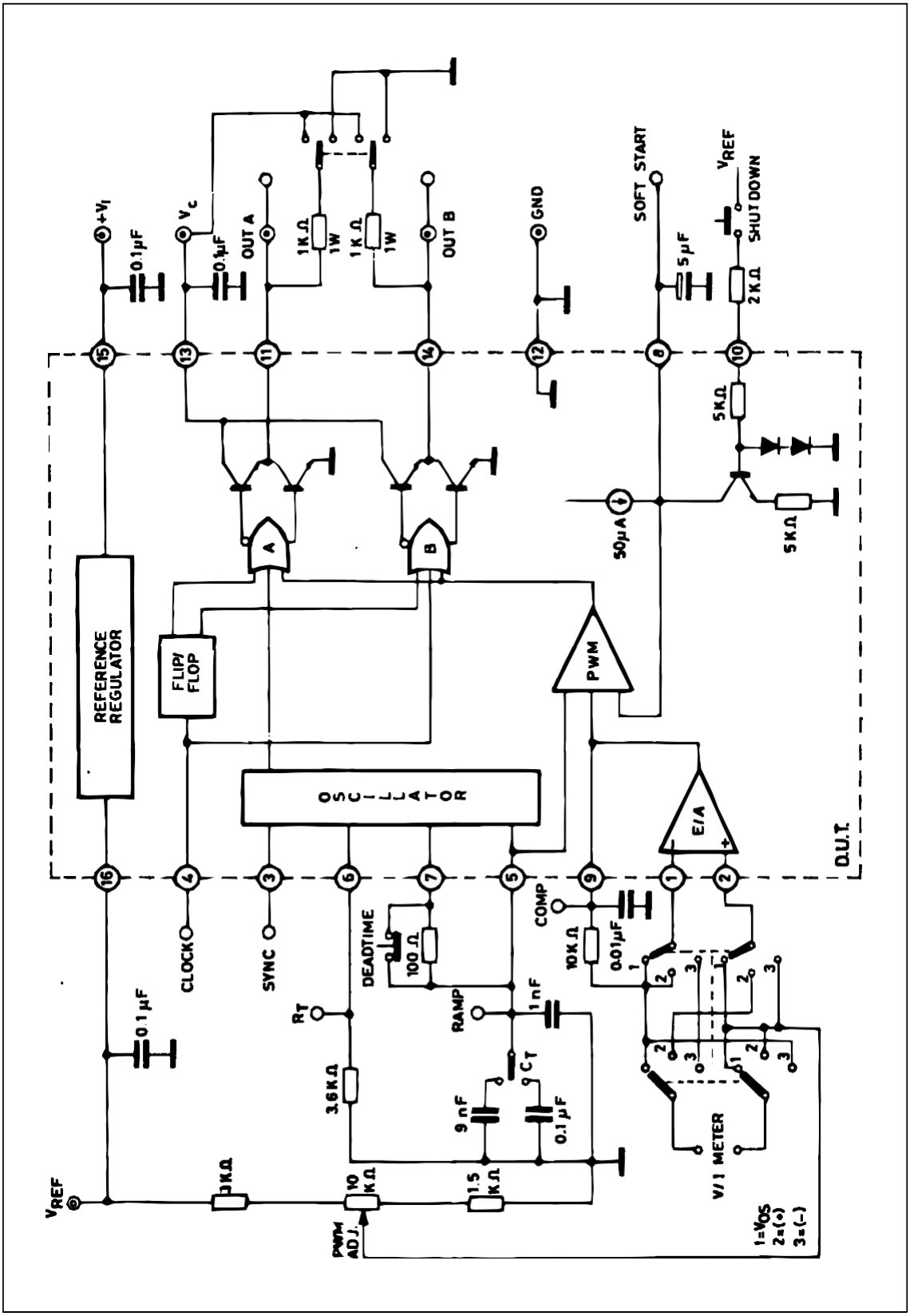
* These parameters, although guaranteed over the recommended operating conditions, are not 100 % tested in production.

• Tested at fosc = 40 KHz (RT = 3.6 K , CT = 10nF, RD = 0). Approximate oscillator frequency is defined by :

$$f = \frac{1}{C_T(0.7R_T + 3R_D)}$$

■ DC transconductance (g_M) relates to DC open-loop voltage gain (G_v) according to the following equation : $G_v = g_M R_L$ where R_L is the resistance from pin 9 to ground. The minimum g_M specification is used to calculate minimum G_v when the error amplifier output is loaded.

TEST CIRCUIT



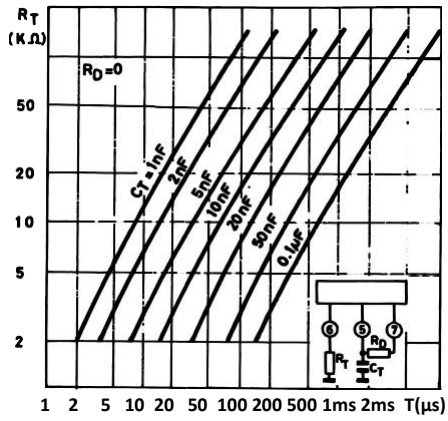


Figure 1 : Oscillator Charge Time vs. RT and CT.

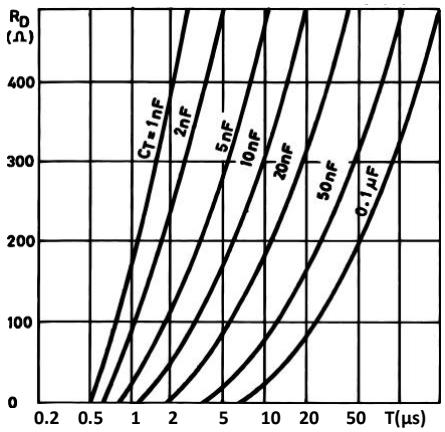


Figure 2 : Oscillator Discharge Time vs. RD and CT.

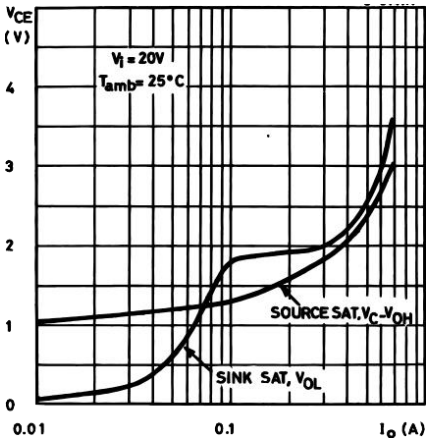


Figure 3 : Output Saturation Characteristics.

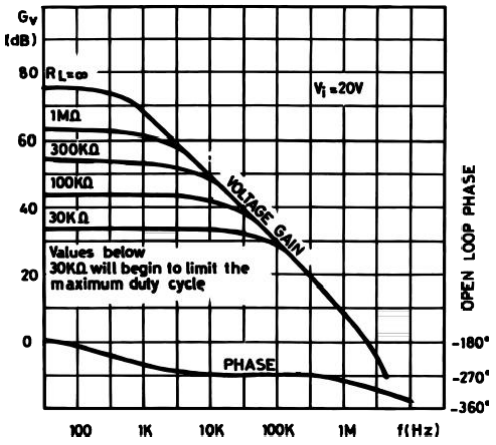


Figure 4 : Error Amplifier Voltage Gain and Phase vs. Frequency.

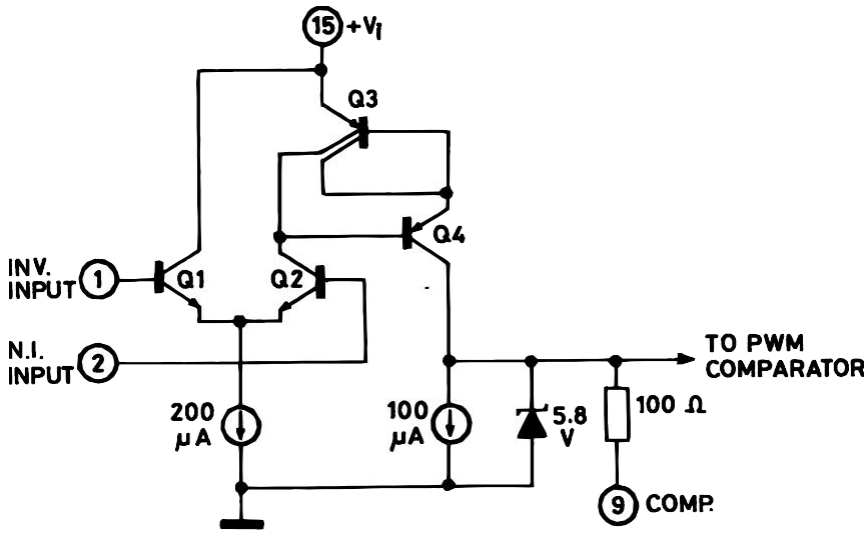


Figure 5 : Error Amplifier.

6. PRINCIPLES OF OPERATION

SHUTDOWN OPTIONS (see Block Diagram)

Since both the compensation and soft-start terminals (Pins 9 and 8) have current source pullups, either can readily accept a pull-down signal which only has to sink a maximum of 100 μA to turn off the outputs. This is subject to the added requirement of discharging whatever external capacitance may be attached to these pins.

An alternate approach is the use of the shutdown circuitry of Pin 10 which has been improved to enhance the available shutdown options. Activating this circuit by applying a positive signal on Pin 10 performs two functions : the PWM latch is immediately set providing the fastest turn-off signal to the outputs ; and a 150 μA current sink begins to dis- charge the external soft-start capacitor. If the shutdown command is short, the PWM signal is terminated without significant discharge of the soft-start capacitor, thus, allowing, for example, a convenient implementation of pulse-by-pulse current limiting. Holding Pin 10 high for a longer duration, however, will ultimately discharge this external capacitor, recycling slow turn-on upon release.

Pin 10 should not be left floating as noise pickup could conceivably interrupt normal operation.

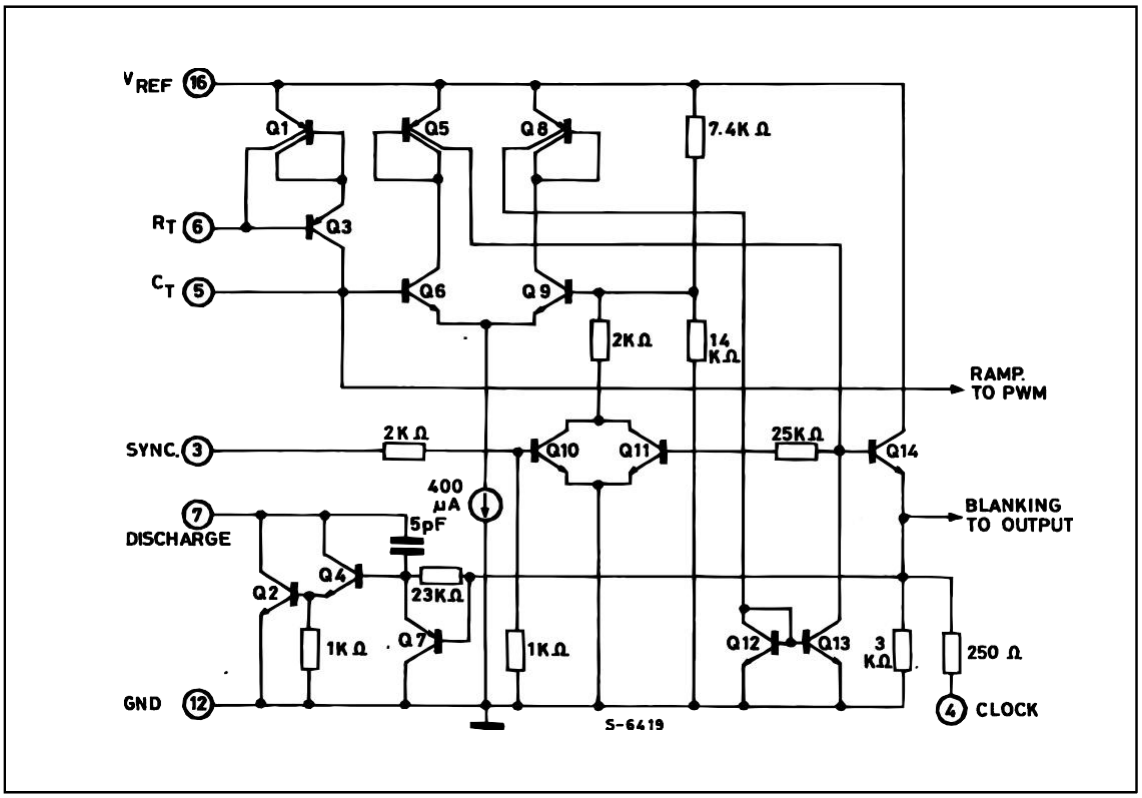


Figure 6-1 : Oscillator Schematic.

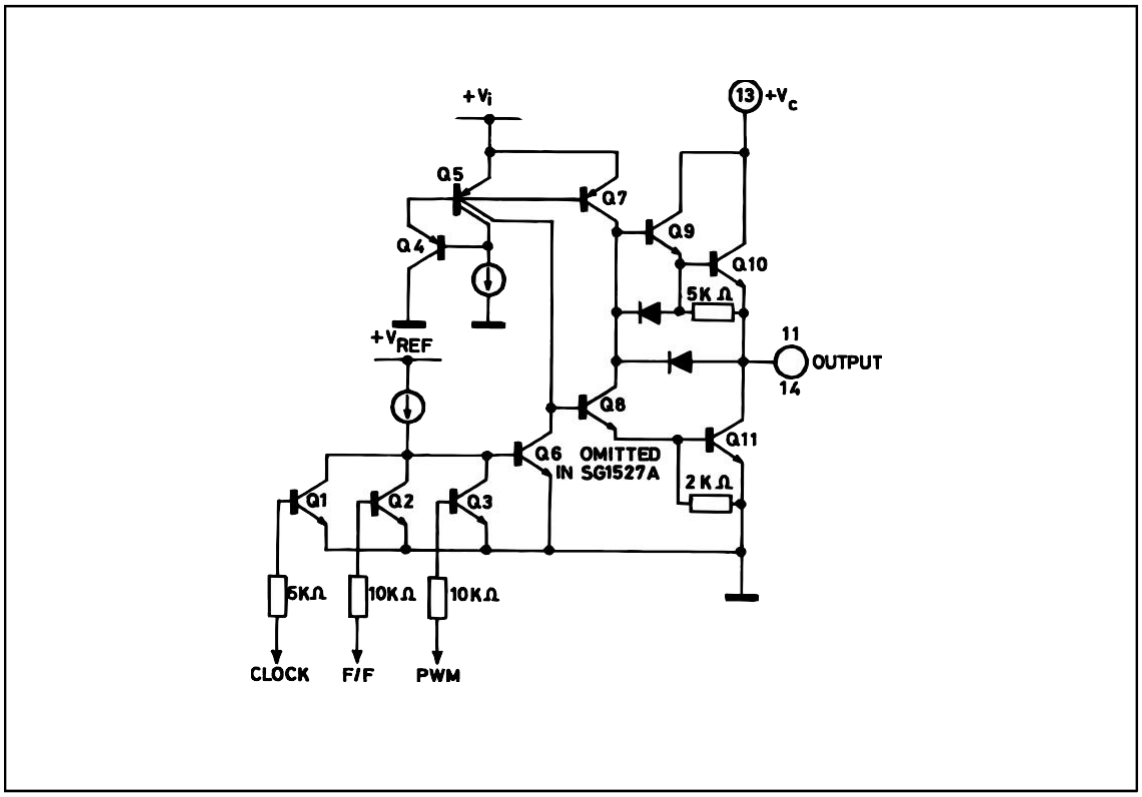


Figure 6-2 : Output Circuit (1/2 circuit shown).

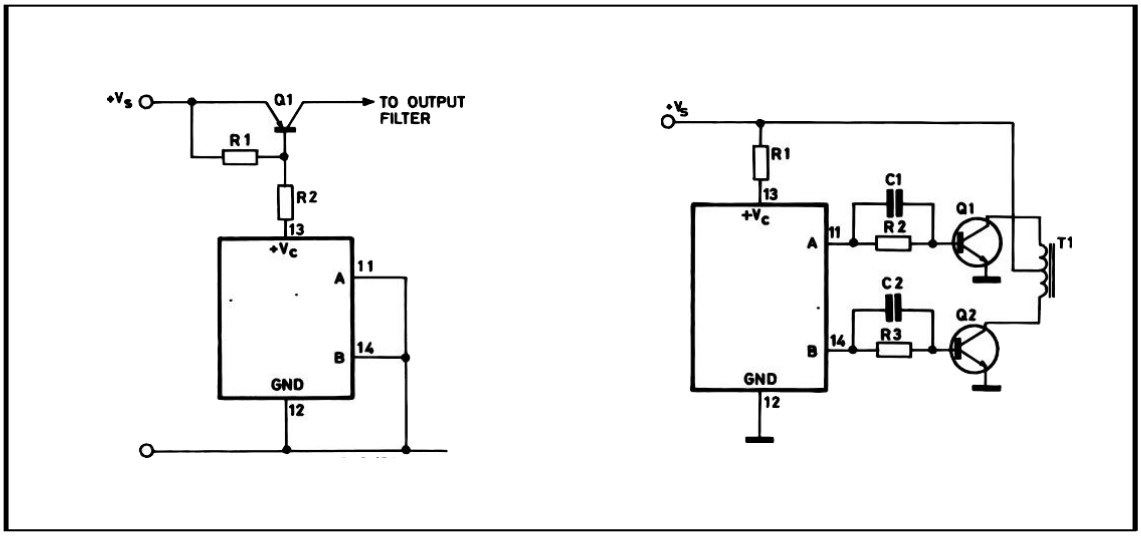


Figure 6-3

For single-ended supplies, the driver outputs are grounded. The VC terminal is switched to ground by the totem-pole source transistors on alternate oscillator cycles.

Figure 6-4

In conventional push-pull bipolar designs, forward base drive is controlled by R1 - R3. Rapid turn-off times for the power devices are achieved with speed-up capacitors C1 and C2.

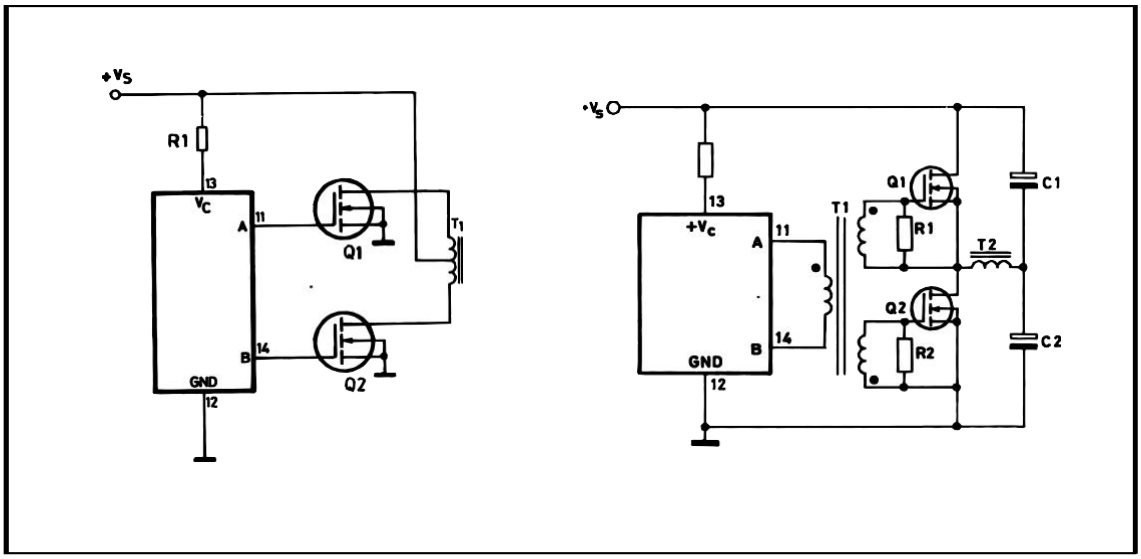


Figure 6-5

The low source impedance of the output drivers provides rapid charging of Power Mos input capacitance while minimizing external components.

Figure 6-6

Low power transformers can be driven directly. Automatic reset occurs during dead time, when both ends of the primary winding are switched to ground.

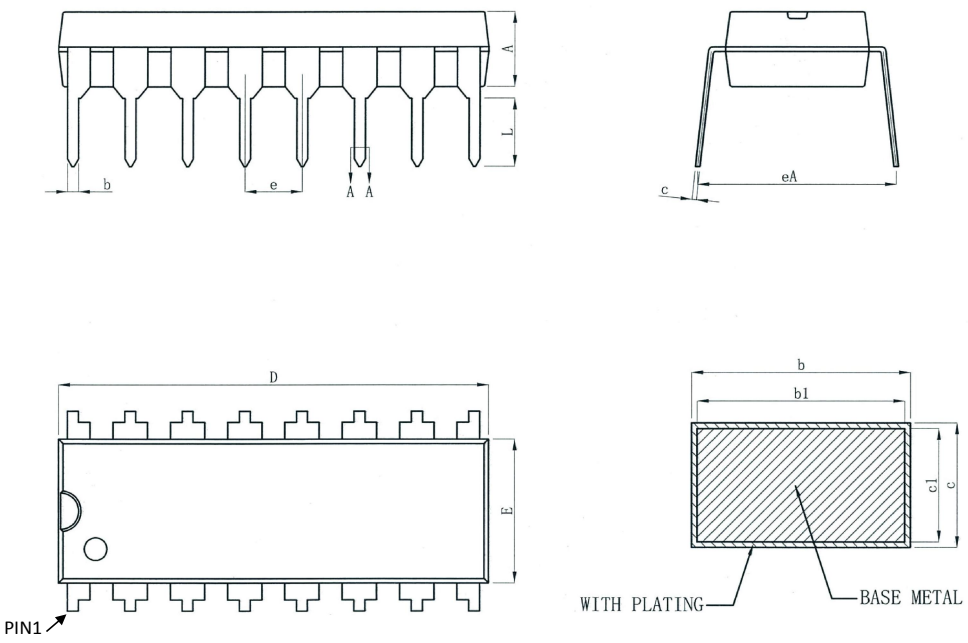
7. ORDERING INFORMATION

Ordering Information

Part Number	Device Marking	Package Type	Body size (mm)	Temperature (°C)	MSL	Transport Media	Package Quantity
XL2525Z	XL2525Z	SOP16	10.00 * 3.95	-40 to +85	MSL3	T&R	1000
XL2525K	XL2525K	SOP16(W)	10.45 * 7.5	-40 to +85	MSL3	T&R	1000
XD2525	XD2525	DIP16	19.05 * 6.35	-40 to +85	MSL3	Tube 25	1000
XL3525Z	XL3525Z	SOP16	10.00 * 3.95	-40 to +85	MSL3	T&R	1000
XL3525K	XL3525K	SOP16(W)	10.45 * 7.5	-40 to +85	MSL3	T&R	1000
XD3525	XD3525	DIP16	19.05 * 6.35	-40 to +85	MSL3	Tube 25	1000

8. DIMENSIONAL DRAWINGS

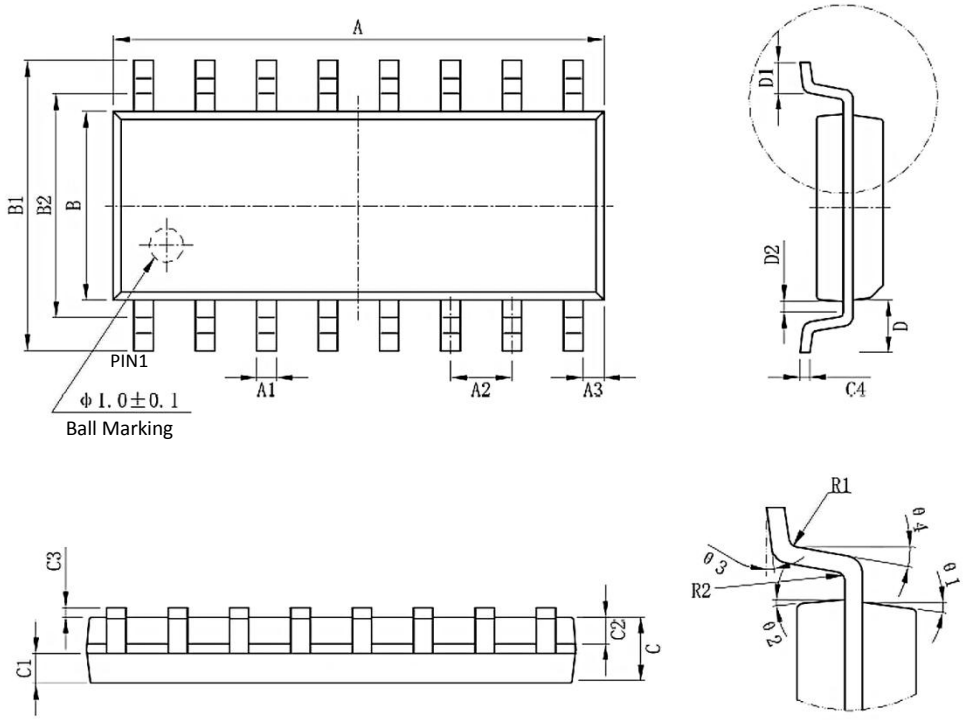
DIP16



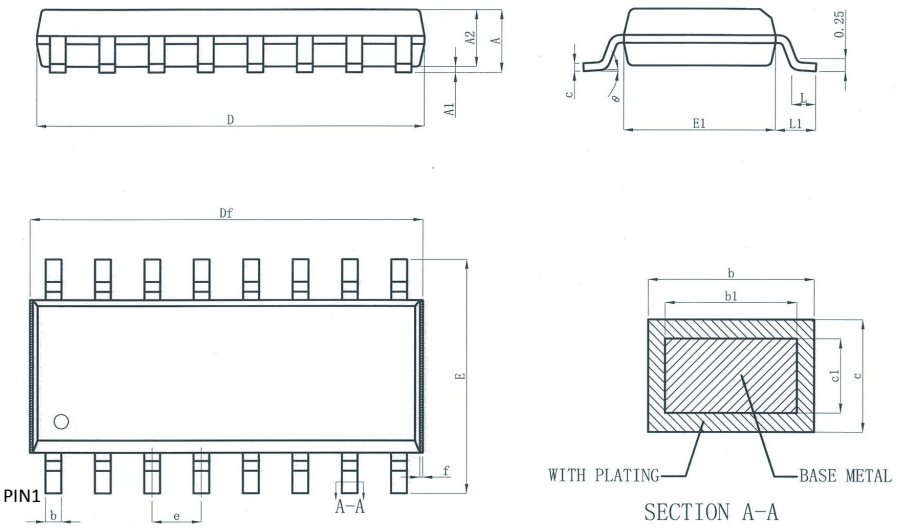
symbol	millimeter		
	Min	Nom	Max
A	3.20	3.30	3.40
b	0.44	---	0.53
b1	0.43	0.46	0.49
c	0.25	---	0.30
c1	0.24	0.25	0.26
D	18.95	19.05	19.15
E	6.25	6.35	6.45
e	2.54BSC		
eA	8.30	8.80	9.30
L	3.00	---	---

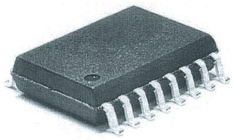
SOP16

Size / Mark	Min (mm)	Max (mm)	Size / Mark	Min (mm)	Max (mm)
A	9.80	10.00	C4	0.203	0.233
A1	0.356	0.456	D	1.05TYP	
A2	1.27TYP		D1	0.40	0.70
A3	0.302TYP		D2	0.15	0.25
B	3.85	3.95	R1	0.20TYP	
B1	5.84	6.24	R2	0.20TYP	
B2	5.00TYP		θ1	8° ~ 12° TYP4	
C	1.40	1.60	θ2	8° ~ 12° TYP4	
C1	0.61	0.71	θ3	0° ~ 8°	
C2	0.54	0.64	θ4	4° ~ 12°	
C3	0.05	0.25			



SOP16(W)





symbol	millimeter		
	Min	Nom	Max
A	---	---	2.65
A1	0.10	0.20	0.30
A2	2.20	2.30	2.40
b	0.39	---	0.47
b1	0.38	0.41	0.43
c	0.25	---	0.30
c1	0.24	0.25	0.26
D	10.10	10.20	10.30
Df	10.20	---	10.70
E	10.26	10.41	10.60
E1	7.40	7.50	7.60
e	1.27BSC		
L	0.55	---	0.85
L1	---	1.40	---
θ	0°	---	8°
f	0.05	---	0.20