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XD3846 DIP-16 XL3846 SOP-16

1 Features

- Automatic Feedforward Compensation
- Programmable Pulse-by-Pulse Current Limiting
- Automatic Symmetry Correction in Push-Pull Configuration
- Enhanced Load Response Characteristics
- Parallel Operation Capability for Modular Power Systems
- Differential Current Sense Amplifier with Wide Common Mode Range
- Double-Pulse Suppression
- 500-mA (Peak) Totem-pole Outputs
- ±1% Band Gap Reference
- Undervoltage Lockout
- Soft-Start Capability
- Shutdown Terminal
- 500-kHz Operation

2 Applications

- Telecommunication Power Converters
- Industrial Power Converters

3 Description

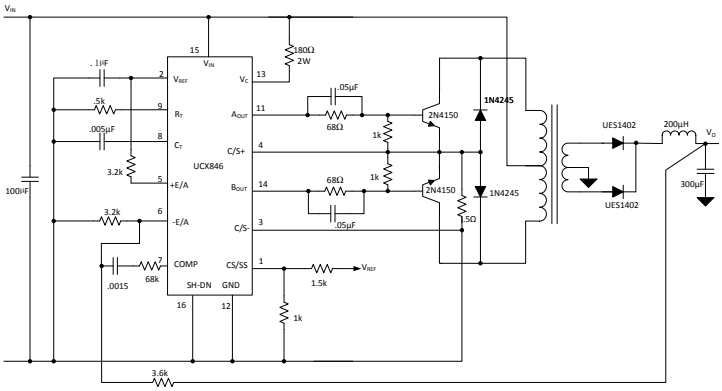
The 1846/7 family of control devices provides all of the necessary features to implement fixed-frequency, current-mode control schemes while maintaining a minimum external parts count. The superior performance of this technique can be measured in improved line regulation, enhanced load response characteristics, and a simpler, easier-to-design control loop. Topological advantages include inherent pulse-by-pulse current limiting capability, automatic symmetry correction for push-pull converters, and the ability to parallel *power modules* while maintaining equal current sharing.

Protection circuitry includes built-in undervoltage lockout and programmable current limit, in addition to soft-start capability. A shutdown function is also available, which can initiate either a complete shutdown with automatic restart or latch the supply off.

Other features include fully-latched operation, double-pulse suppression, deadline adjust capability, and a ±1% trimmed band gap reference.

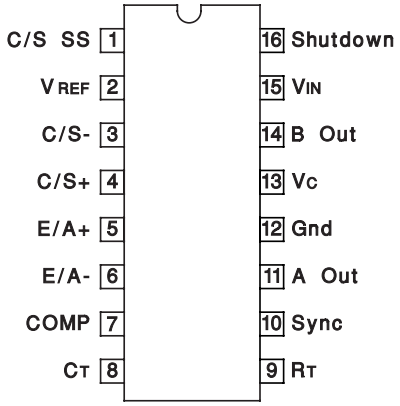
The 1846 features low outputs in the OFF state, while the 3846 features high outputs in the OFF state.

4 Block Diagram



5 Pin Configuration and Functions

J or N, DW Packages
16-Pin CDIP or PDIP, SOIC
Top View



Pin Functions

PIN			I/O	DESCRIPTION
DIL, SOIC NO.	PLCC, LCC NO.	NAME		
1	2	C/S SS	I	Current limit/soft-start programming
2	3	V_{REF}	O	5.1-V reference voltage output
3	4	C/S –	I	Current sense comparator inverting input
4	5	C/S +	I	Current sense comparator non-inverting input
5	7	E/A +	I	Error amplifier inverting input
6	8	E/A –	I	Error amplifier inverting input
7	9	COMP	I/O	Error amplifier output and input to the PWM comparator
8	10	C_T	I	Oscillator frequency programming capacitor pin
9	12	C_R	I	Oscillator frequency programming resistor pin
10	13	Sync	I/O	Synchronization out from master controller or input of slave controller
11	14	A Out	O	PWM drive signal output A, Pin11 and P14 are complementary
12	15	GND	G	All signals are referenced to this node
13	17	V_C	I	Bias supply input for output stage
14	18	B Out	O	PWM drive signal output B, Pin11 and P14 are complementary
15	19	V_{IN}	I	Bias supply input
16	20	Shutdown	I	External shutdown signal input
—	1, 6, 11, 16	N/C		

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

	MIN	MAX	UNIT
Supply Voltage (Pin 15)		40	V
Collector Supply Voltage (Pin 13)		40	V
Output Current, Source or Sink (Pins 11, 14)		500	mA
Analog Inputs (Pins 3, 4, 5, 6, 16)	–0.3	$+V_{IN}$	V
Reference Output Current (Pin 2)		–30	mA
Sync Output Current (Pin 10)		–5	mA
Error Amplifier Output Current (Pin 7)		–5	mA
Soft Start Sink Current (Pin 1)		50	mA
Oscillator Charging Current (Pin 9)		5	mA
Power Dissipation at T_A = 25°C		1000	mW
Power Dissipation at T_C = 25°C		2000	mW
Storage temperature, T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$ Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2500	V
	Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	NOM	MAX	UNIT
VREF terminal external capacitance	1		2.2	µF

6.4 Thermal Information

THERMAL METRIC(1)		3846		UNIT
		N or DW (PDIP or SOIC)	J or DW (CDIP or SOIC)	
		16 PINS	16 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	41.8	73.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	28.5	34.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	21.8	38.0	°C/W
ψ_{JT}	Junction-to-top characterization parameter	13.0	7.7	°C/W
ψ_{JB}	Junction-to-board characterization parameter	21.7	37.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	°C/W

6.5 Electrical Characteristics

T_A=–55°C to +125°C for 1846/7; –40°C to +85°C for the 2846/7; and 0°C to +70°C for the 3846; V_{IN}=15 V, R_T=10k, C_T=4.7 nF, T_A=T_J (unless otherwise noted)

PARAMETER	TEST CONDITIONS	1846/7 2846/7			XD/XL3846			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
REFERENCE								
Output Voltage	T_J = 25°C, I_O = 1 mA	5.05	5.10	5.15	5.00	5.10	5.20	V
Line Regulation	V_{IN} = 8 V to 40 V		5	20		5	20	mV
Load Regulation	I_L = 1 mA to 10 mA		3	15		3	15	mV
Temperature Stability	Over Operating Range, (1)		0.4			0.4		mV/°C
Total Output Variation	Line, Load, and Temperature (1)	5.00		5.20	4.95		5.25	V
Output Noise Voltage	10 Hz ≤ f ≤10 kHz, T_J = 25°C(1)		100			100		µV
Long Term Stability	T_J = 125°C, 1000 Hrs(1)		5			5		mV
Short Circuit Output Current	V_{REF} = 0 V	–10	–45		–10	–45		mA
OSCILLATOR								
Initial Accuracy	T_J = 25°C	39	43	47	39	43	47	kHz
Voltage Stability	V_{IN} =8 V to 40 V		–1%	2%		–1%	2%	
Temperature Stability	Over Operating Range (1)		–1%			–1%		
Sync Output High Level		3.9	4.35		3.9	4.35		V
Sync Output Low Level			2.3	2.5		2.3	2.5	V
Sync Input High Level	Pin 8 = 0 V	3.9			3.9			V
Sync Input Low Level	Pin 8 = 0 V			2.5			2.5	V
Sync Input Current	Sync Voltage = 3.9 V, Pin 8 = 0 V		1.3	1.5		1.3	1.5	mA
ERROR AMPLIFIER								
Input Offset Voltage			0.5	5		0.5	10	mV
Input Bias Current			–0.6	–1		–0.6	–2	µA
Input Offset Current			40	250		40	250	nA
Common Mode Range	V_{IN} = 8 V to 40 V	0		V_{IN} - 2 V	0		V_{IN} - 2 V	V
Open Loop Voltage Gain	ΔV_O = 1.2 to 3 V, V_{CM} = 2 V	80	105		80	105		dB
Unity Gain Bandwidth	T_J = 25°C(1)	0.7	1.0		0.7	1.0		MHz
CMRR	V_{CM} = 0 V to 38 V, V_{IN} = 40 V	75	100		75	100		dB
PSRR	V_{IN} = 8 V to 40 V	80	105		80	105		dB
Output Sink Current	V_{ID} = –15 mV to -5 V, V_{PIN7} = 1.2 V	2	6		2	6		mA
Output Source Current	V_{ID} = 15 mV to -5 V, V_{PIN7} = 2.5 V	–0.4	–0.5		–0.4	–0.5		mA
High Level Output Voltage	R_L = (Pin 7) 15 kΩ	4.3	4.6		4.3	4.6		V
Low Level Output Voltage	R_L = (Pin 7) 15 kΩ		0.7	1		0.7	1	V
CURRENT SENSE AMPLIFIER								
Amplifier Gain	$V_{PIN\ 3}$ = 0 V, Pin 1 Open(2), (3)	2.5	2.75	3.0	2.5	2.75	3.0	V

(1) These parameters, although ensured over the recommended operating conditions, are not 100% tested in production.
(2) Parameter measured at trip point of latch with VPIN 5 = VREF, VPIN 6 = 0 V.
(3) Amplifier gain defined as: G = ΔV_{PIN7} / ΔV_{PIN4}; V_{PIN4} = 0 to 1.0 V

Electrical Characteristics (continued)

T_A=–55°C to +125°C for 1846/7; –40°C to +85°C for the 2846/7; and 0°C to +70°C for the 3846; V_{IN}=15 V, R_T=10k, C_T=4.7 nF, T_A=T_J (unless otherwise noted)

PARAMETER	TEST CONDITIONS	1846/7 2846/7			XD/XL3846			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
Maximum Differential Input Signal ($V_{PIN\ 4}$-$V_{PIN\ 3}$)	Pin 1 Open (2); R_L (Pin 7) = 15 kW	1.1	1.2		1.1	1.2		V
Input Offset Voltage	$V_{PIN\ 1}$ = 0.5 V, Pin 7 Open(2)		5	25		5	25	mV
CMRR	V_{CM} = 1 V to 12 V	60	83		60	83		dB
PSRR	V_{IN} = 8 V to 40 V	60	84		60	84		dB
Input Bias Current	$V_{PIN\ 1}$ = 0.5 V, Pin 7 Open(2)		–2.5	–10		–2.5	–10	µA
Input Offset Current	$V_{PIN\ 1}$ = 0.5 V, Pin 7 Open(2)		0.08	1		0.08	1	µA
Input Common Mode Range		0		V_{IN}-3	0		V_{IN}-3	V
Delay to Outputs	T_J = 25°C (1)		200	500		200	500	ns
CURRENT LIMIT ADJUST								
Current Limit Offset	$V_{PIN\ 3}$ = 0 V, $V_{PIN\ 4}$ = 0 V, Pin 7 Open (2)	0.45	0.5	0.55	0.45	0.5	0.55	V
Input Bias Current	$V_{PIN\ 5}$ = V_{REF}, $V_{PIN\ 6}$ = 0 V		–10	–30		–10	–30	µA
SHUTDOWN TERMINAL								
Threshold Voltage		250	350	400	250	350	400	mV
Input Voltage Range		0		V_{IN}	0		V_{IN}	V
Minimum Latching Current (I_{PIN1})		(4)3.0	1.5		3.0	1.5		mA
Maximum Latching Current (I_{PIN1})			(5)1.5	0.8		1.5	0.8	mA
Delay to Outputs	T_J = 25°C (1)		300	600		300	600	ns
OUTPUT								
Collector-Emitter Voltage		40			40			V
Collector Leakage Current	V_C = 40 V (6)			200			200	µA
Output Low Level	I_{SINK} = 20 mA		0.1	0.4		0.1	0.4	V
	I_{SINK} = 100 mA		0.4	2.1		0.4	2.1	
Output High Level	I_{SOURCE} = 20 mA	13	13.5		13	13.5		V
	I_{SOURCE} = 100 mA	12	13.5		12	13.5		
Rise Time	C_L = 1 nF, T_J = 25°C (1)		50	300		50	300	ns
Fall Time	C_L = 1 nF, T_J = 25°C (1)		50	300		50	300	ns
UNDERVOLTAGE LOCKOUT								
Start-Up Threshold			7.7	8.0		7.7	8.0	V
Threshold Hysteresis			0.75			0.75		V
TOTAL STANDBY CURRENT								
Supply Current			17	21		17	21	mA

(4) Current into Pin 1 ensured to latch circuit in shutdown state.
(5) Current into Pin 1 ensured not to latch circuit in shutdown state.
(6) Applies to 1846/2846/3846 only due to polarity of outputs.

6.6 Typical Characteristics

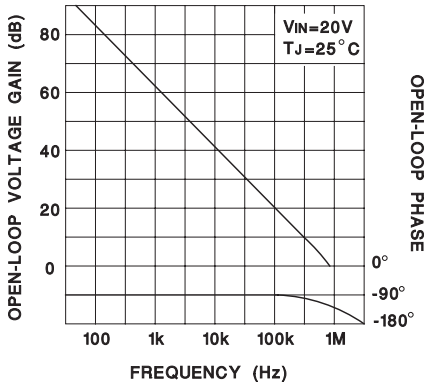


Figure 1. Error Amplifier Gain and Phase vs Frequency

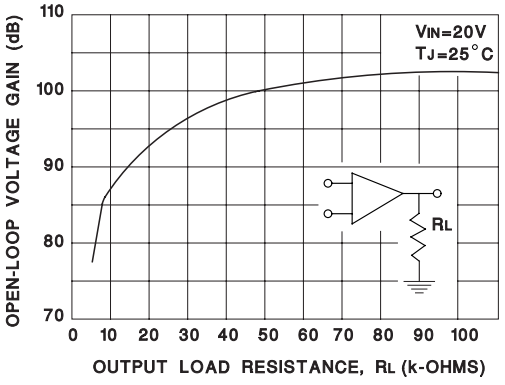


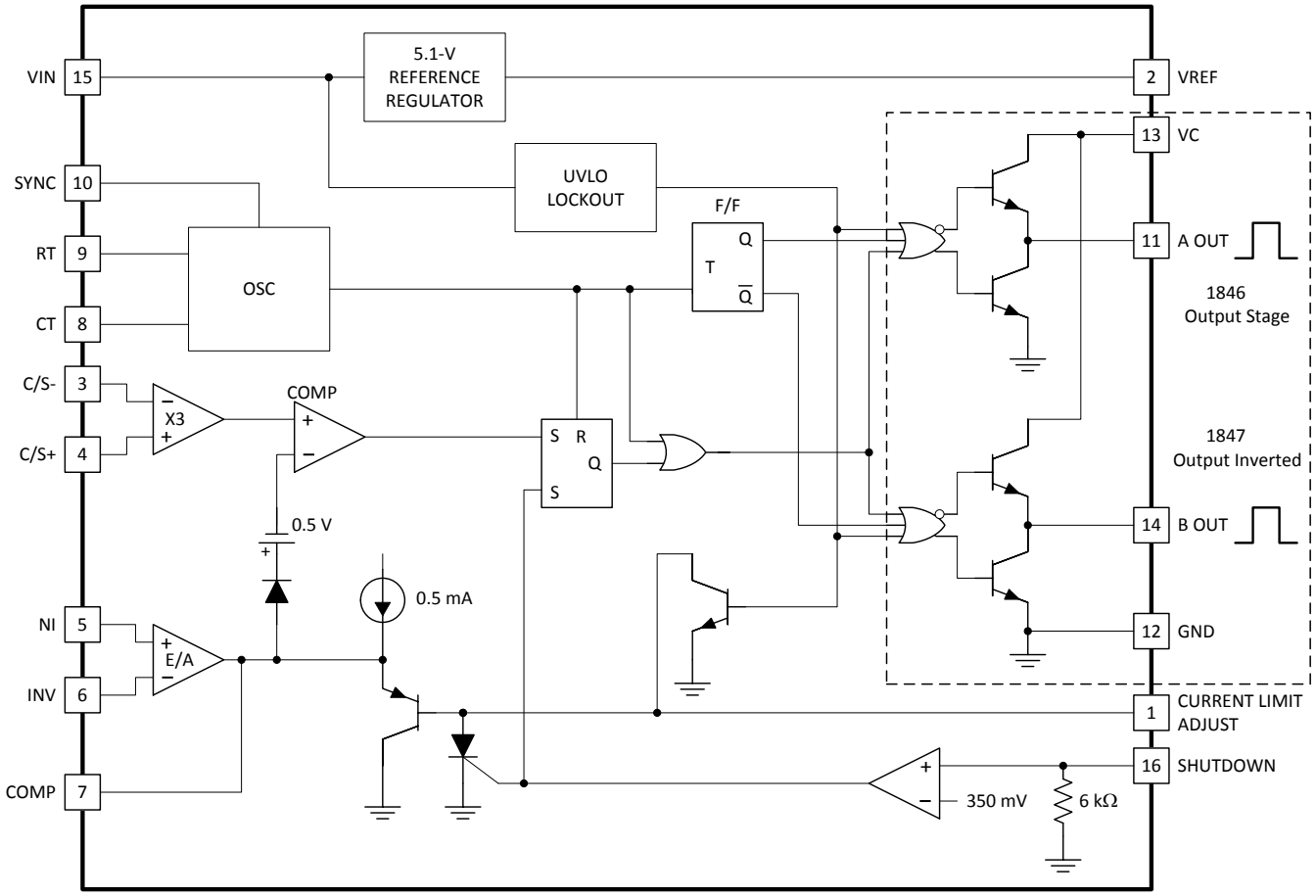
Figure 2. Error amplifier Open-Logic DC Gain vs Load Resistance

7 Detailed Description

7.1 Overview

The 3846 family of control devices provides the necessary features to implement off-line or DC-to-DC fixed-frequency, current-mode control schemes with a minimal external parts count. Internally implemented circuits include under-voltage lockout featuring start-up current less than 1 mA, a precision reference trimmed for accuracy at the error amplifier input, logic to insure latched operation, a PWM comparator which also provides current limit control, and a totem pole output stage designed to source or sink high-peak current. The output stage, suitable for driving either N-Channel MOSFETs or bipolar transistor switches, is low in the off state.

7.2 Functional Block Diagram

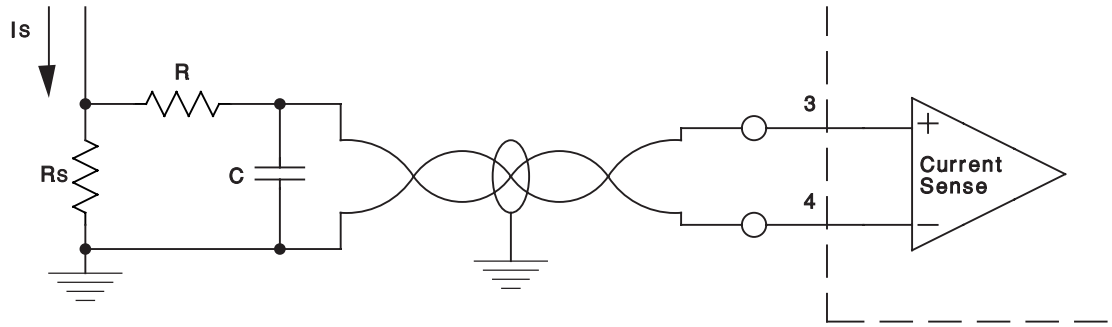


7.3 Feature Description

7.3.1 Current Sense Amplifier

The current sense amplifier may be used in a variety of ways to sense peak switch current for comparison with an error voltage. Referring to *Functional Block Diagram*, maximum swing on the inverting input of the PWM comparator is limited to approximately 3.5 V by the internal regulated supply. Accordingly, for a fixed gain of 3, maximum differential voltages must be kept below 1.2 V at the current sense inputs.

Feature Description (continued)



A small RC filter may be required in some applications to reduce switch transients. Differential input allows remote, noise free sensing.

Figure 3. Current Sense Amplifier Connection

7.3.2 Oscillator

By implementing the oscillator using all NPN transistors, the 3846 achieves excellent temperature stability and waveform clarity at frequencies in excess of 1 MHz.

Referring to Figure 4, an external resistor R_T is used to generate a constant current into a capacitor C_T to produce a linear sawtooth waveform. Oscillator frequency may be approximated by selecting R_T and C_T such that:

$$f_{OSC} = \frac{2.2}{R_T C_T} \quad (1)$$

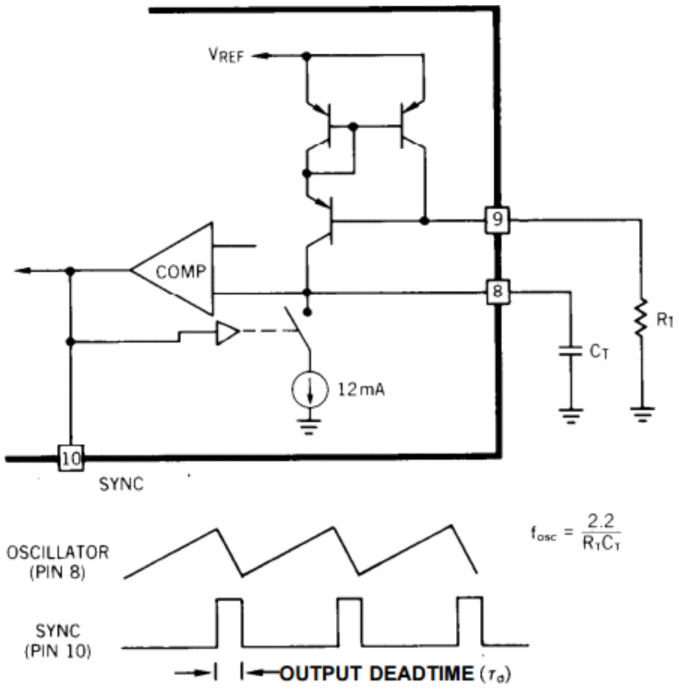


Figure 4. Oscillator Circuit

8 Application and Implementation

8.1 Application Information

The 3846 family of control devices provides all of the necessary features to implement fixed frequency, current mode control schemes while maintaining a minimum external parts count. The superior performance of this technique can be measured in improved line regulation, enhanced load response characteristics, and a simpler, easier to design control loop. Topological advantages include inherent pulse-by-pulse current limiting capability, automatic symmetry correction for push-pull converters. Protection circuitry includes undervoltage lockout and programmable current limit in addition to soft-start capability. A shutdown function is also available which initiates either a complete shutdown with automatic restart or latch the supply off.

8.2 Typical Application

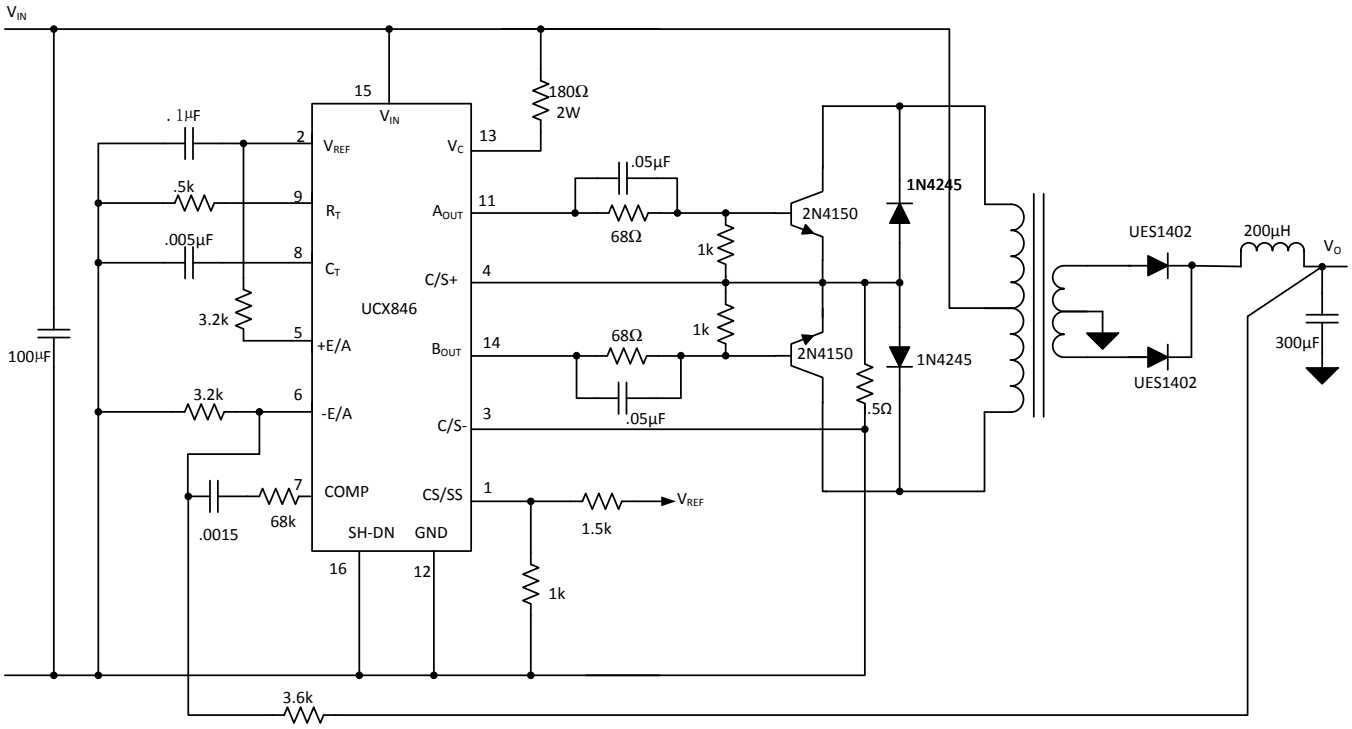


Figure 5. Typical Application Diagram

8.2.1 Design Requirements

Table 1 shows the design parameters for this application.

Table 1. Design Parameters

DESIGN PARAMETER	TARGET VALUE
Typical efficiency	85%
Switching frequency	880 kHz
Pulse by pulse current limit threshold	1 A

8.2.2 Detailed Design Procedure

This section details the design procedure based on the design requirements.

8.2.2.1 Design Switching Frequency

Output deadtime is determined by the external capacitor, C_T, according to the formula:

$$Td(\mu s) = 145\,C_T(\mu F)\left[\frac{ID}{ID - \frac{3.6}{RT(k\Omega)}}\right]$$

where

- ID = Oscillator discharge current at 25°C; typically is 7.5.

For large values of R_T: τd (μs) ≈145CT (μF).

Oscillator frequency is approximated by the formula:

$$fT(kHz) \approx \frac{2.2}{\left(R_T(k\Omega) \times C_T(\mu F)\right)}$$

8.2.2.2 Error Amplifier Output Configuration

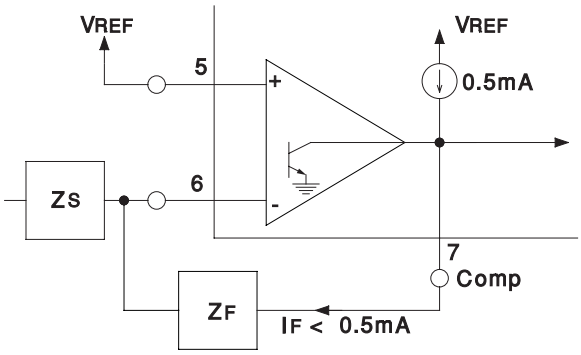
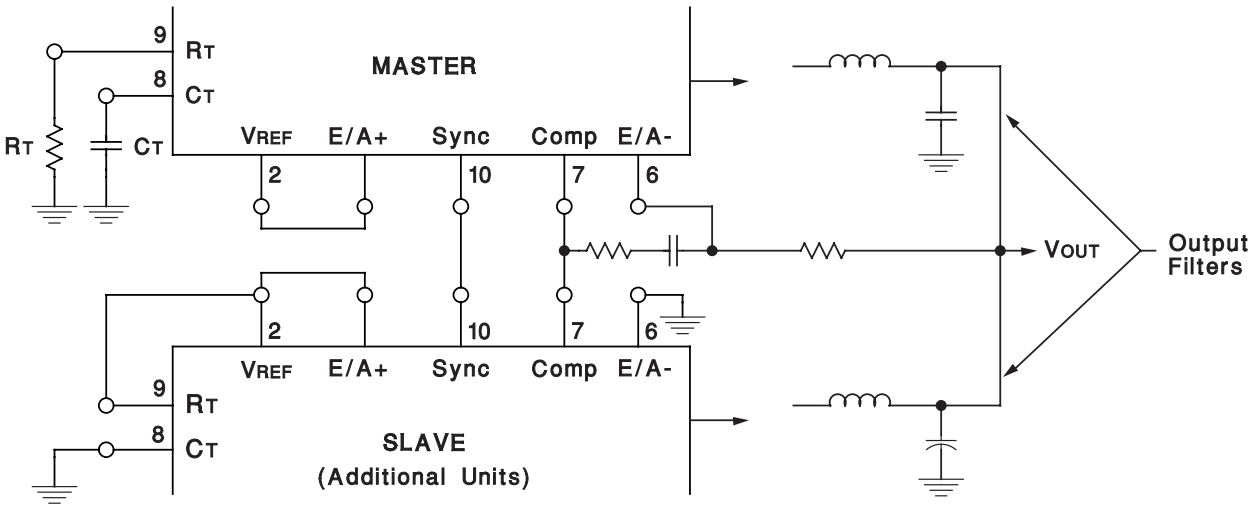


Figure 6. Error Amplifier Output Configuration

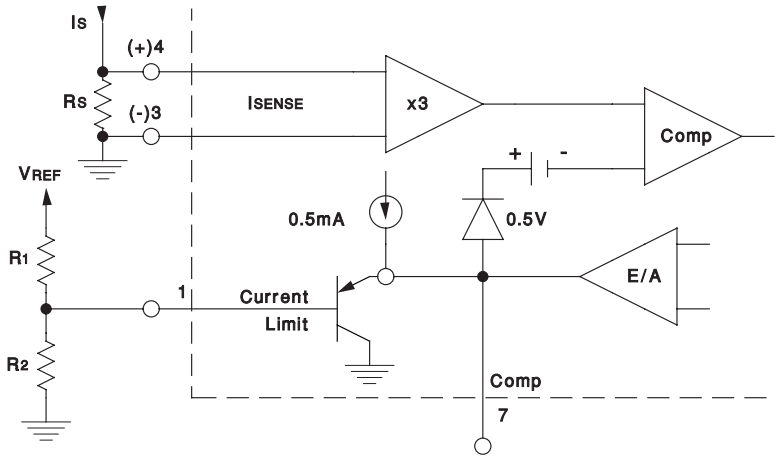
8.2.2.3 Parallel Operation Configuration



Slaving allows parallel operation of two or more units with equal current sharing.

Figure 7. Parallel Operation

8.2.2.4 Design Pulse by Pulse Current Limit Threshold



Peak Current (Is) is determined by the formula: $IS = \dfrac{\dfrac{R2\,VREF}{R1 + R2} - 0.5}{3RS}$

Figure 8. Pulse by Pulse Current Limiting

8.2.2.5 Soft-Start and Shutdown, Restart Function Design

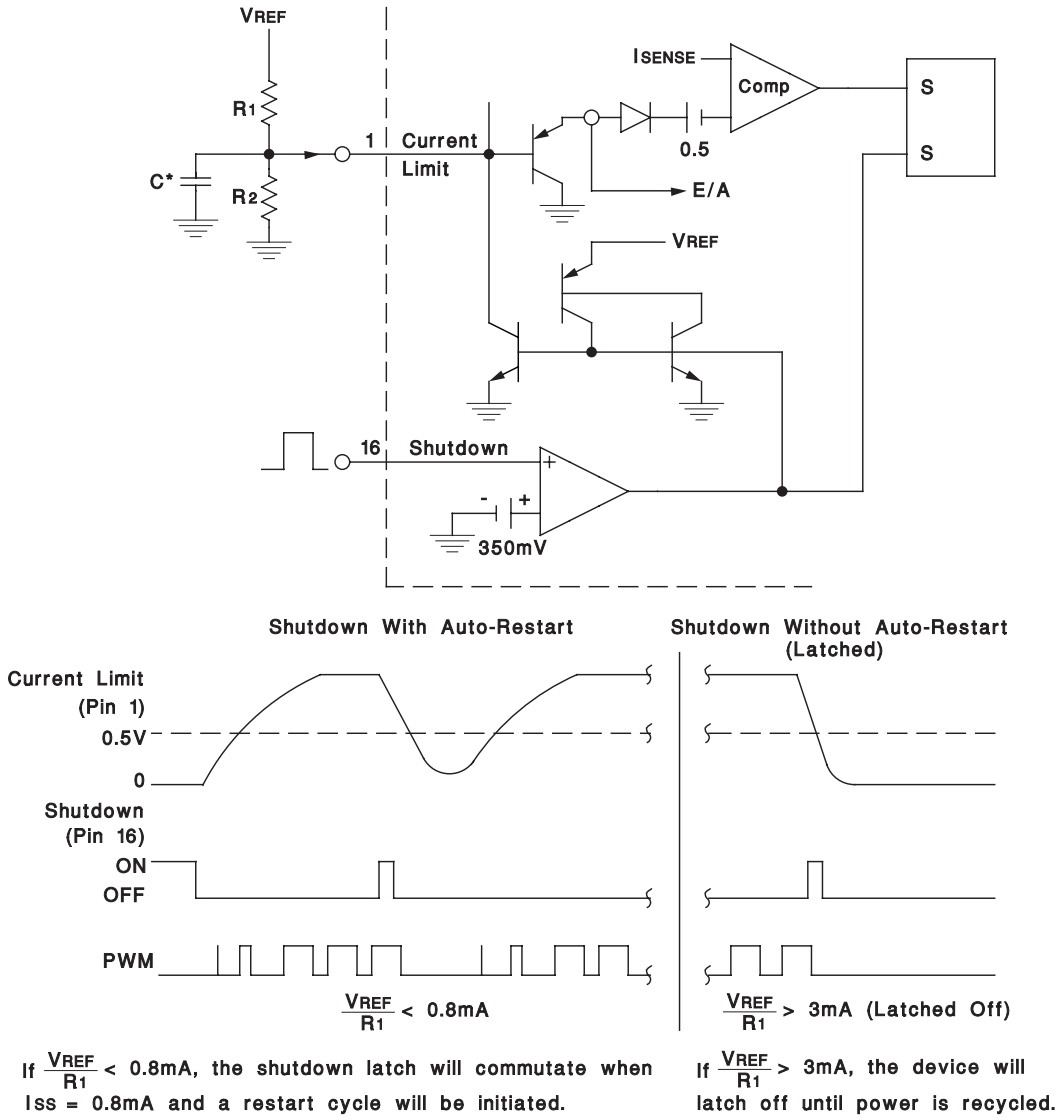


Figure 9. Soft-Start and Shutdown, Restart Functions

9 Layout

9.1 Layout Guidelines

- Place a low ESR and ESL decoupling capacitor C_{REF} in the 1-µF to 2.2-µF range, preferably ceramic, from VREF pin to GND.
- The EA+ is a non-inverting input, the EA– is an inverting input and the COMP is the output of the error amplifier. Place resistor and capacitor series network between EA+ pin and COMP pin, and reduce the trace of resistor and capacitor series network as much as possible.
- Place a low ESR and ESL capacitor C_T, preferably ceramic, from CT pin to GND, and place C_T close to 3846 as much as possible.
- Place a resistor R_T from RT pin to GND, and place R_T close to UCx846/7 as much as possible.

9.2 Layout Example

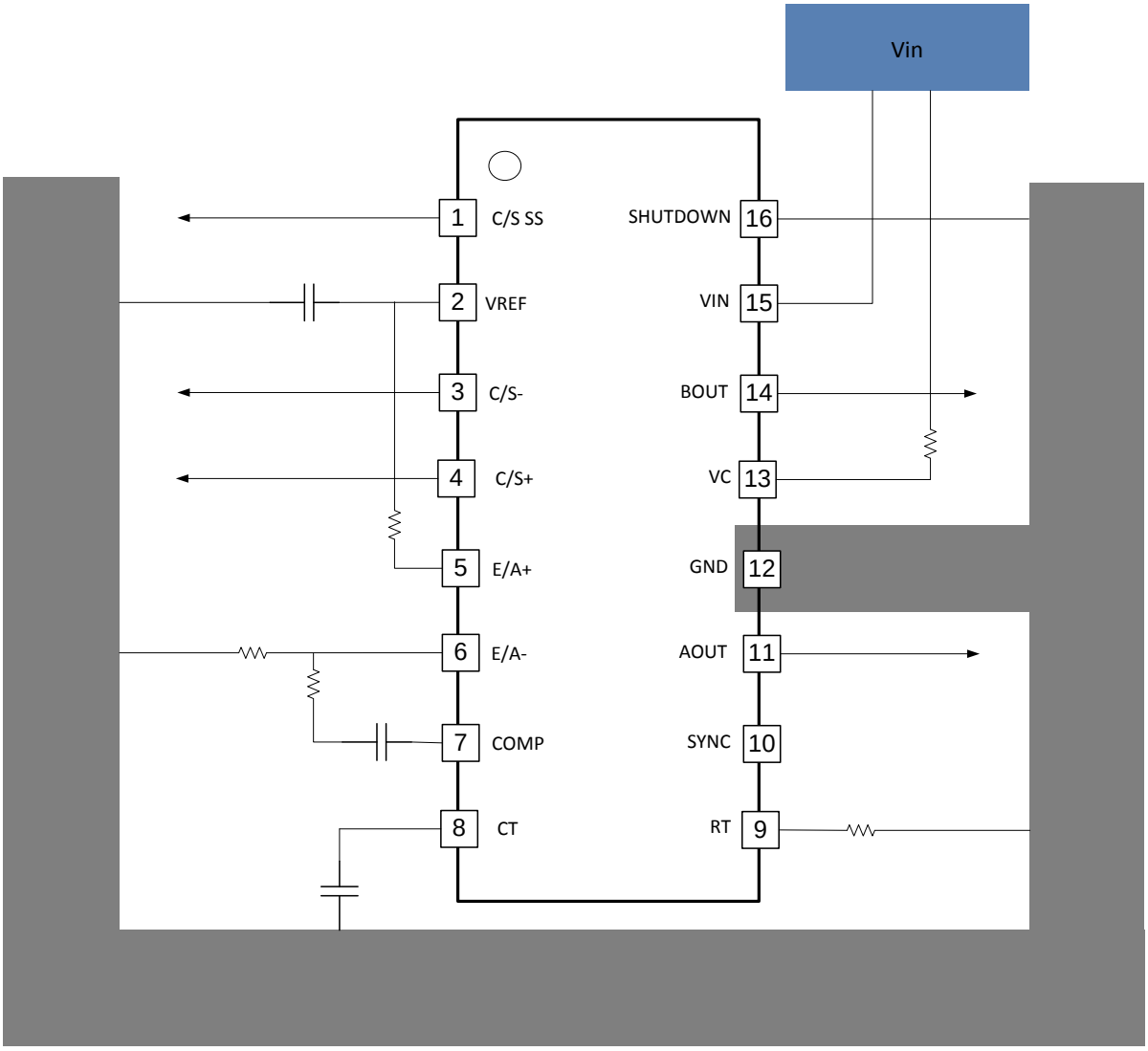


Figure 10. 3846 Layout Example